HR_C6000 User Manual

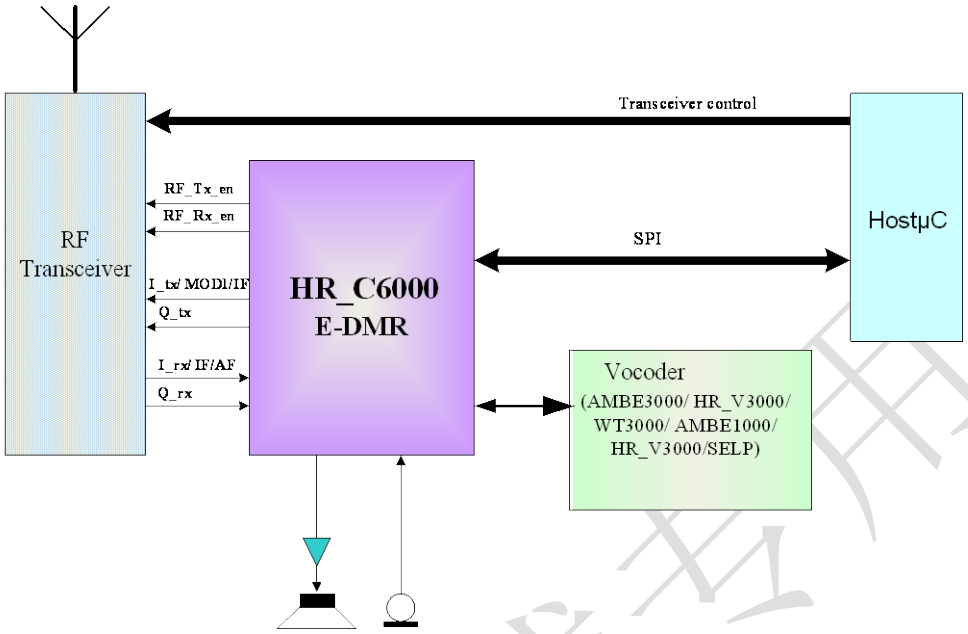
repair Book

Edit Brief description of the revised content		Revision date	Revised edition This number	Reviser Reviewer Approver		
1	create	2013.12.03	A0	Cai Jinen Chen Hudong Chen Hudong		
2	increase Reg0x55 Definition of registers 2014.02.26		A1	Cai Jinen Chen Hudong Chen Hudong		
3	Modify the analog clock configuration, the digital and analog related clock	2014.04.26 A2		Cai Jinen Chen Hudong Chen Hudong		

characteristic

- DMR
  - meets the ETSI TS102 361 (DMR) Tier I / II / III Standard protocol design
  - Support physical layer, data link layer and call control layer independent control
  - Support true dual time slot sync header detection
  - use TDMA Technology, supporting full-duplex, half-duplex voice, data communication and digital simultaneous interpretation services
  - stand by IP Data service
  - Support single frequency, dual frequency relay
  - stand by 4.8Kbps with 9.6Kbps data transmission
  - Support digital analog intelligent detection
  - Support relay voice and data function
  - Support voice encryption
- Modulation and demodulation and channel codec
  - high performance 4FSK Modem
  - Channel codec specified by the integration protocol
- Vocoder support
  - stand by HR_V3000 (Hongrui AMBE + 2) , SELP Vocoder (Tsinghua), AVDS Vocoder (712) Wait SPI The vocoder of the interface provides an interface for digital recording, playback and prompt sound input at the same time
  - Seamless AMBE3000 , AMBE1000 , WT3000 Wait for the vocoder, by HR_C6000 Automatically complete the configuration of the vocoder and the control of the interactive data with the vocoder
  - Support digital voice encryption
- RF interface
  - Transmitting RF interface adopts single-ended output and supports baseband IQ , Intermediate frequency, two-point modulation
  - Receive radio frequency interface adopts differential input mode, supports baseband IQ , IF and AF
  - Send two signals offset, amplitude can be adjusted independently
  - Support user configuration GPIO Control RF channel
- simulation FM
  - stand by 12.5KHz / 25KHz Channel communication
  - Support weighting and de-weighting
  - Support compression and decompression
  - stand by CDCSS / CTCSS Subtone processing
  - stand by 2-tone / 5-tone deal with
  - stand by DTMF deal with
  - Support analog squelch function
  - stand by MSK Modulation and demodulation
- Built-in high performance IP
  - high performance ADC / DAC
  - DC-DC ,use 3.3V powered by
  - high performance PLL
  - high performance Codec , Supports differential or single-ended Mic Enter and Line_out Output
- Support external Codec I^2S interface
- Adopt low power consumption design, the typical working power consumption of the chip is less than 40mW
- use LQFP-80 Package

Application Block Diagram



Introduction

Hong Rui independently developed HR_C6000 Chip compliance ETSI TS102 361 (DMR) Digital intercom standard, while supporting digital PDT Cluster intercom, analog intercom and analog cluster intercom applications are terminal chips for positioning high-end applications.

Chip integrated high performance 4FSK modem, MSK Modem, analog intercom channel, sub audio, DTMF , 2-Tone , 5-Tone The simulation function, channel coding and decoding, protocol processor, etc. adopt the layered design of physical layer, data link layer and call control layer. DMR The development of standard digital interphone greatly reduces the workload of development and shortens the development time; users can also HR_C6000 On the basis of a layer 2 protocol PDT protocol, DMR TierIII Or the development of custom protocols to meet the needs of high-end users. The chip is suitable for digital intercom consoles, dedicated trunk terminals and low-speed data and voice transmission terminal applications, and supports relay and central terminal applications.

Built-in chip AD / DA , CodeC , DC-DC Wait for multiple IP , Effectively reduce the user's peripheral devices; at the same time, can be seamlessly docked AMBE3000 , WT3000 , AMBE1000 , HR_V3000 , SELP , AVDS Various vocoders, support two-point modulation transmission, low intermediate frequency reception, compatible with the original analog radio frequency channel, reduce the workload of user RF development

Chip adoption 3.3V Power supply, built-in power management module to achieve low power design.

Products for users LQFP-80 Package.

table of Contents

1 Chip block diagram

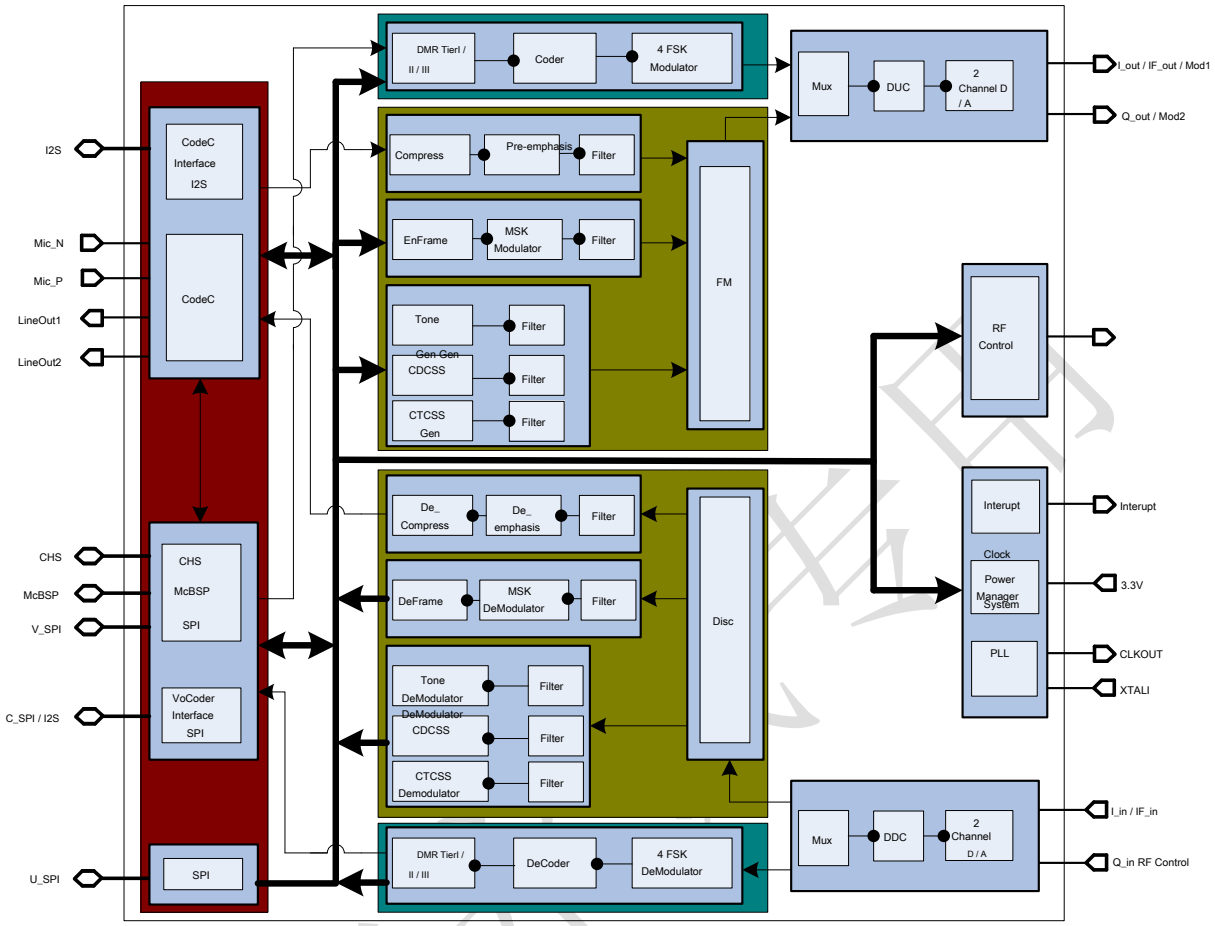


Fig 1.1 HR_C6000 Block diagram of the internal structure of the chip

2 Chip pin

2.1 Pin diagram

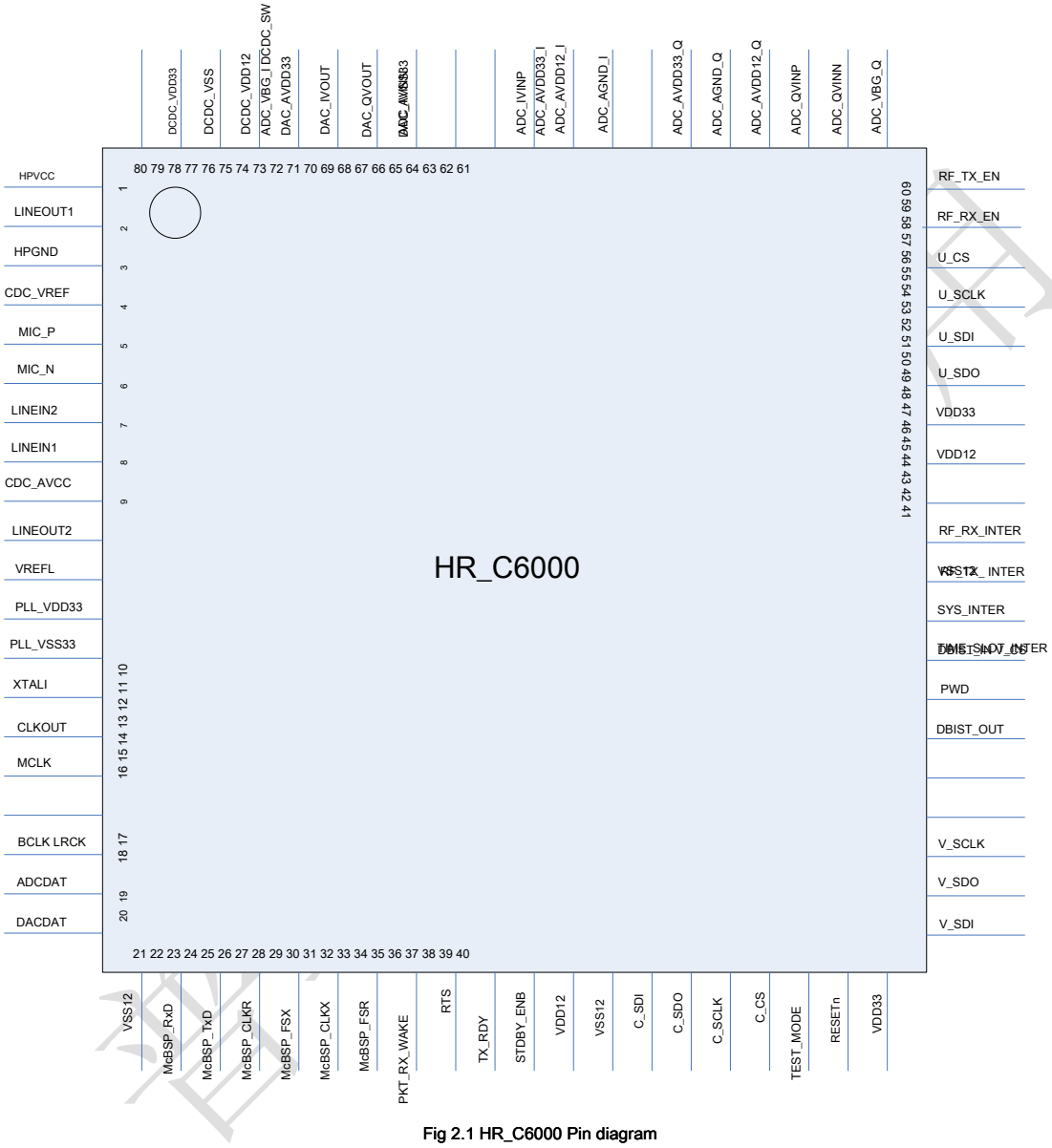


Fig 2.1 HR_C6000 Pin diagram

2.2 Pin list

table 2.1 Pin arrangement

diagram	Pin name	Type pin description	
1	HPVCC	AP	Headphone output amplifier simulation 3.3V power supply.
2	LINEOUT1	AO Headphone output.	

3	HPGND	AG	Built-in Codec Analog ground.
4	CDC_VREF	AO	Built-in Codec Reference power supply.
5	MIC_P	AI	The positive end of the microphone differential input.
6	MIC_N	AI	The negative terminal of the microphone differential input.
7	LINEIN1	AI	Microphone single-ended input 1 .
8	LINEIN2	AI	Microphone single-ended input 2 .
9	CDC_AVCC	AP	Codec simulation 3.3V power supply.
10	LINEOUT2	AO	Line-out Output, need to add external power amplifier drive.
11	VREFL	AG	The external reference negative terminal of the microphone is connected to the analog ground.
12	PLL_VDD33	AP	PLL simulation 3.3V power supply.
13	PLL_VSS33	AG	PLL Analog ground.
14	XTALI	DI	System clock, active crystal input.
15	CLKOUT	DO	HR_C6000 Output clock by PLL The output clock is divided by the frequency division ratio reg0xBB Configuration. Available for external Codec Or use an external vocoder.
16	MCLK / RF_ANT_EN	DIO	External Codec Interface working clock, the clock consists of CLKOUT Provided, if external Codec Do not use CLKOUT , The clock needs to use an external Codec Working clock; also multiplexed as the digital control enable of the RF transmitter, in this case, the output characteristics.
17	LRCK / RF_3TC_EN	DO	External Codec Left and right channel selection enable; multiplexing Enable digital control as the RF transmitter.
18	BCLK / RF_3RC_EN	DO	External Codec Bit clock; multiplexed as radio frequency Digital control at the receiving end is enabled.
19	ADCDAT / RF_5TC_EN	DIO	External Codec Audio ADC Sampling data; multiplexing As the digital control of the RF transmitter is enabled, this is the output characteristic.
20	DACDAT / RF_5RC_EN	DO	External Codec Audio DAC Data; reuse as Digital control is enabled on the RF receiver.
twenty one	VSS12	G	Core digitally.
twenty two	McBSP_RxD / CHS_DI	DO	AMBE3000 : HR_C6000 by McBSP Interface sent to AMBE3000 The data; AMBE1000 : HR_C6000 by CHS Serial port sent to AMBE1000 Frame input data.
twenty three	McBSP_TxD / CHS_DO	DI	AMBE3000 : HR_C6000 by McBSP Interface receive AMBE3000 Sent data; AMBE1000 : HR_C6000 by CHS Serial port reception AMBE1000 Frame output data.
twenty four	McBSP_CLKR / CHS_O_CLK	DO	AMBE3000 : HR_C6000 of McBSP Interface output clock; AMBE1000 : AMBE1000 of CHS interface

			clock.
25	McBSP_FSX	DI	AMBE3000 : HR_C6000 by McBSP Interface receive AMBE3000 Output data synchronization signal.
26	McBSp_CLKX	DI	AMBE3000 : HR_C6000 of McBSP Interface input clock.
27	McBSP_FSR / CHS_I_STRB	DO	AMBE3000 : HR_C6000 by McBSP Interface sent to AMBE3000 Data synchronization signal; AMBE1000 : CHS_DI Port data is effectively enabled.
28	PKT_RX_WAKE / CHS_O_STRB	DO	AMBE3000 :will McBSP_FSR Reverse, used to wake up McBSP interface; AMBE1000 : CHS_DO Port data is effectively enabled.
29	RTS / DPE	DI	AMBE3000 : AMBE3000 Allow to pass McBsp Interface write data, low effective; AMBE1000 : AMBE1000 The decoding packet is empty.
30	TX_RDY / EPR	DI	AMBE3000 : AMBE3000 The data packet is ready to be completed, highly efficient; AMBE1000 : AMBE1000 Encoding package is ready.
31	STDBY_ENB / RESET_AMBE1000	DO	AMBE3000 : AMBE3000 Standby Mode enable, high level effective; AMBE1000 : AMBE1000 of RESET , Low effective.
32	VDD12	P	Core number 1.2V power supply.
33	VSS12	G	Core digitally.
34	C_SDI / I2S_RX	DI	As SPI When interface: connect vocoder SPI Serial data input to HR_C6000 , SPI Work in main mode. As I2S Interface: can work in master / slave mode. If working in master mode, read from vocoder PCM Serial data to HR_C6000 ; If working in slave mode, the vocoder will PCM Data is written to HR_C6000 .
35	C_SDO / I2S_TX	DO	As SPI When connecting: HR_C6000 will CodecADC The voice data of the terminal is output to the vocoder SPI port. As I2S Interface: can work in master / slave mode. If working in master mode, HR_C6000 will PCM The data is written into the vocoder for compression coding; if it works in slave mode, the vocoder HR_C6000 Read PCM The data is encoded.

36	C_SCLK / I2S_CK	DO / DI	As SPI When interface: Vocoder SPI Serial clock. As I2S Interface: can work in master / slave mode. If working in the main mode, if working in the main mode, the I2S Master clock; if working in slave mode, provides the vocoder to HR_C6000 of I2S Interface working clock
37	C_CS / I2S_FS	DO / DI	As SPI When interface: Vocoder SPI Selection of mouth. As I2S Interface: can work in master / slave mode. If working in the main mode, provide read and write to the vocoder I2S Enable left and right channel data; if working in slave mode, the vocoder provides HR_C6000 The left and right channels of reading and writing serial data are enabled.
38	TEST_MODE	DI	Test mode configuration pins, 1 For test mode, 0 It is the normal working mode.
39	RESETn	DI	System reset signal, active low.
40	VDD33	P	digital IO 3.3V power supply.
41	V_SDI	DI	Universal Vocoder SPI Serial data input.
42	V_SDO	DO Universal Vocoder SPI Serial data output.	
43	V_SCLK	DI	Universal Vocoder SPI Serial clock.
44	V_CS	DI	Universal Vocoder SPI Port selection signal.
45	DBIST_IN	DI	None, input ground.
46	DBIST_OUT	DO no.	
47	PWD	DI	chip PowerDown Control pin, high level PowerDown status.
48	TIME_SLOT_INTER	DO	30ms The time slot is interrupted.
49	SYS_INTER	DO System control is interrupted.	
50	RF_TX_INTER	DO The radio terminal sends relevant parameter configuration interrupts, such as sending Send mixer frequency point configuration.	
51	RF_RX_INTER	DO The radio frequency terminal receives relevant parameter configuration interruption, such as receiving Receive mixer frequency point configuration.	
52	VSS12	G	Core digitally.
53	VDD12	P	Core number 1.2V power supply.
54	VDD33	P	digital IO 3.3V power supply.
55	U_SDO	DO	MCU access HR_C6000 Register or RAM Store SPI Data output.
56	U_SDI	DI	MCU access HR_C6000 Register or RAM Store SPI data input.
57	U_SCLK	DI	MCU access HR_C6000 Register or RAM Store SPI Serial clock.

58	U_CS	DI	MCU access HR_C6000 Register or RAM Store SPI Chip Select.
59	RF_RX_EN	DO	Control the radio frequency receiving switch to be enabled, and output high level in the receiving state. The signal will not RF_TX_EN Also effective.
60	RF_TX_EN	DO	Control the radio frequency transmission switch to be enabled, and output high level in the transmission state. The signal will not RF_RX_EN Also effective.
61	ADC_VBG_Q	AIO	Q road ADC Bandgap voltage for decoupling outside the channel.
62	ADC_QVINN	AI	Q road ADC The negative terminal of the channel differential input.
63	ADC_QVINP	AI	Q road ADC The positive end of the channel's differential input.
64	ADC_AVDD12_Q	AP	Q road ADC Channel simulation 1.2V power supply.
65	ADC_AGND_Q	AG	Q road ADC Channel analog ground.
66	ADC_AVDD33_Q	AP	ADC simulation 3.3V power supply.
67	ADC_AVDD33_I	AP	ADC simulation 3.3V power supply.
68	ADC_AGND_I	AG	I road ADC Channel analog ground.
69	ADC_AVDD12_I	AP	I road ADC Channel simulation 1.2V power supply.
70	ADC_IVINP	AI	I road ADC The positive terminal of the channel differential input, or the signal access terminal in the intermediate frequency receiving mode.
71	ADC_IVINN	AI	I road ADC The negative terminal of the channel differential input. This port is grounded or other fixed voltage in IF receiving mode.
72	ADC_VBG_I	AIO	I road ADC Bandgap voltage for decoupling outside the channel.
73	DAC_AVSS33	AG	DAC Analog ground.
74	DAC_QVOUT / MOD2	AO	Q road DAC Channel output signal, or in two-point modulation transmission mode MOD2 port.
75	DAC_IVOUT / MOD1	AO	I road DAC Channel output signal, or in two-point modulation transmission mode MOD1 port.
76	DAC_AVDD33	AP	DAC simulation 3.3V power supply.
77	DCDC_VDD12	AO	DC-DC 1.2V Output.
78	DCDC_VSS	G	DC-DC Digitally.
79	DCDC_VDD33	P	DC-DC 3.3V power supply.
80	DCDC_SW	O	DC-DC internal Switch .

2.3 Package size

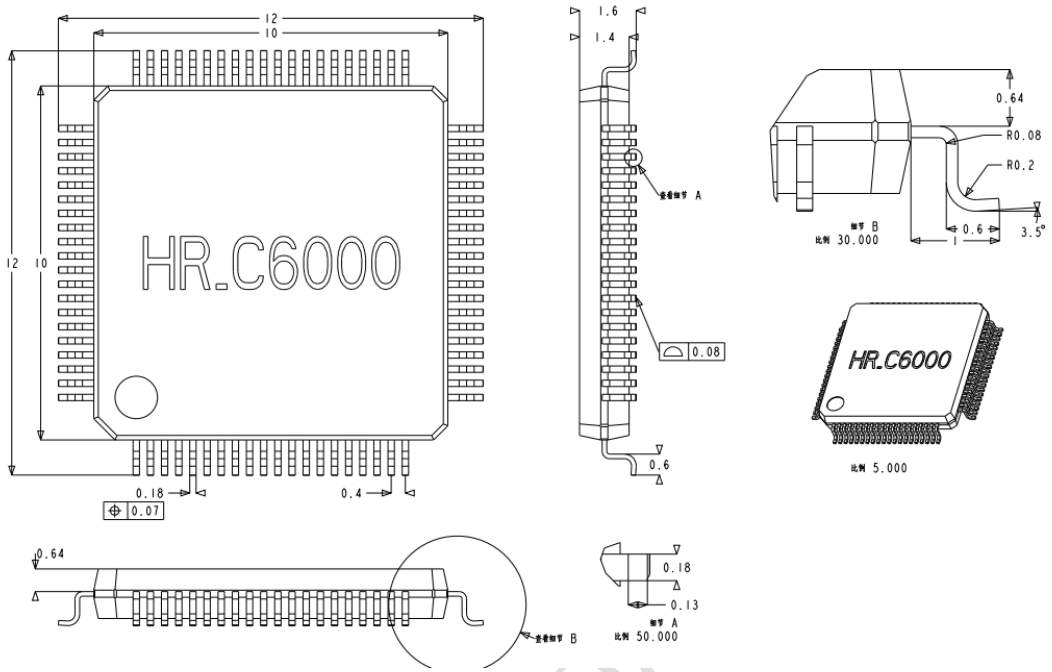


Fig 2.2 Package size diagram

3 Characteristic parameter

3.1 Static characteristics

table 3.1 HR_C6000 Static parameters

parameter	condition Minimum value		Typical value	Maximum	unit
powered by					
VDD33 , VCC		3.0	3.3	3.6	V
VDD12			1.2		V
Operating temperature		-40		85	℃
Input clock					
frequency			12.288		MHz
Clock signal offset			1.5		V
Clock signal amplitude		320			mV_{pp}
DC-DC					
Input voltage		2.7	3.3	5.5	V
The output voltage			1.2		V

Output voltage ripple			50		mV
Output current			100		mA
effectiveness		85			%
ADC					
Resolution			10		Bits
Input voltage	gain = 0		2		V_{ppdif}
	gain = 1		1		V_{ppdif}
Input common mode voltage		0.5	1.25	2	V
Signal bandwidth	-3dB		40		MHz
input resistance			0.5		pF
			1.25		pF
Gain error				± 1.2	% FSR
Offset error				± 2.4	% FSR
DNL			± 0.5		LSB
INL			± 1		LSB
THD			-65		dB
DAC					
Resolution			10		Bits
The output voltage	simulation 3.3V	0.005		3.15	V
Gain error			± 2.5		% FSR
Offset error			± 0.30		% FSR
DNL			± 1.0		LSB
INL			± 1.5		LSB
Resistive load			1.5		KOhm
Capacitive load				30	pF
Codec					
Resolution			16		Bits
Codec middle ADC					
Input voltage				1.6	V_{pp}
input resistance			20		KOhm
THD + N			0.08		%
Passband bandwidth		0		0.42	Fs
Passband ripple				± 0.1	dB
Stop band		0.58			Fs
Stop band attenuation		76			dB
HPOut The output voltage				1.6	V_{pp}
HPOut Load impedance		16			Ohm
LineOut Load impedance		30			KOhm
THD + N			0.05		%

Output pin logic level					
Output " 1 "(I_{OH} =)				2.4	V
Output " 0 "(I_{OL} =)		0.4			V
Input pin logic level					
Enter " 1 "		2.0		5.5	V
Enter " 0 "		-0.3		0.8	V

3.2 Dynamic characteristics

table 3.2 HR_C6000 Static parameters

parameter	condition Minimum value		Typical value	Maximum	unit
DAC					
SNR			57		dB
SINAD			55		dBFS
ADC					
SNR			57		dB
SINAD			56.5		dB
Codec in ADC					
Input voltage SNR			90		dB
LineOut Output SNR			95		dB

3.3 Power consumption parameters

table 3.3 HR_C6000 Power consumption parameters

parameter	condition	Typical value	unit		
Sleep state	Note 1		1.66		mA
Two-point modulation transmission, IF reception					
Standby	Note 2		11.51		mA
Time slot transmission (voice)	Note 2		11.32		mA
Time slot transmission (digital)	Note 2		8.40		mA
Continuous transmission (voice)	Note 2		11.57		mA
Continuous transmission (data)	Note 2		8.64		mA
Time slot reception (voice)	Note 2		11.86		mA
Time slot reception (data)			9.85		mA
Continuous reception (voice)	Note 2		13.44		mA

Continuous reception (data)			11.53		mA
Full duplex	Note 2		13.72		mA

Note 1 : When the software is in the reset state, the chip PWD Was pulled down.

Note 2 : Turn on all the way in standby ADC And all the way DAC , Codec use HR_C6000 Dynamic control.

3.4 Performance parameter

table 3.4 HR_C6000 Modem Performance parameter

parameter	condition	Minimum value	Typical value	Maximum	unit
send					
Two-point modulation (Mod1 / Mod2)					
Signal bias		1.228	1.65	2.072	V
Signal offset adjustment accuracy			3.3		mV
Signal amplitude		8.75		2240	mV
Signal amplitude adjustment accuracy			8.75		mV
IQ modulation(I / Q)					
Signal bias		1.386	1.65	1.914	V
Signal offset adjustment accuracy			3.3		mV
Signal amplitude		0.17		2.725	V
Signal amplitude adjustment accuracy			0.17		V
receive					
IQ demodulation(I / Q)					
Signal bias		0.5	1.25	2	V
$E_b N_0$	BER = 5%		7		dB
Minimum receiving threshold		130			mV ppdif
IF demodulation					
Signal bias		0.5	1.25	2	V
Receive IF frequency			450k	1M	Hz
$E_b N_0$	BER = 5%		7		dB
Minimum receiving threshold	Noise	150			mV ppdif
Codec					
Mic Gain adjustment		-12		twenty four	dB
Mic Gain adjustment step			3		dB
Digital volume adjustment		-45		45	dB
Digital volume adjustment step			1.5		dB
HPOut Gain adjustment		0		6	dB

4 Application note

4.1 Chip reset

4.1.1 Power-on reset

HR_C6000 Resistors and capacitors can be used for power-on reset. The reference circuit is as follows.

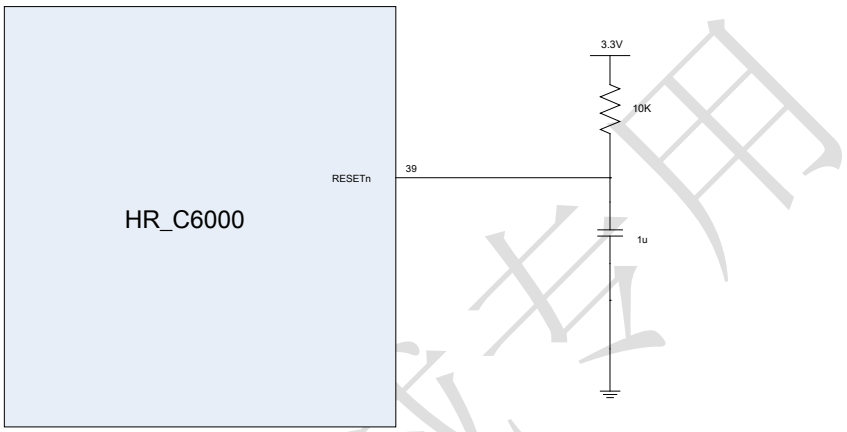


Fig 4.1 Chip power-on reset reference circuit

To ensure successful power-on reset, the reset time is required to be kept to a minimum 0.1μs . as the picture shows, 0-0.8V Is a stable low-level voltage range, 2.0-3.3V It is a stable high-level voltage range.

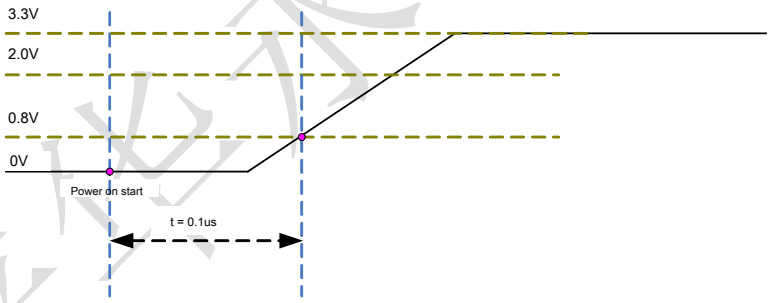


Fig 4.2 Chip power-on reset timing diagram

It is recommended to use CPU The same reset chip or by CPU of GPIO As a reset pin.

4.1.2 Software reset

HR_C6000 In addition to automatically performing the reset process at power-on, it can also be passed according to actual application needs MCU Software reset the chip. Software reset operation through configuration register Reg0x00 of Bit7 achieve. will Reg0x00 of Bit7 Configured as 0 After completing HR_C6000 A soft reset, the reset time is one Sys_Clk Pulse width, ie

$$\frac{1}{9.8304}\ \mu s$$

. The Bit Configured as 0 No need to pass MCU Configure again 1 Return to normal working mode, HR_C6000 Automatically Bit Set 1 .

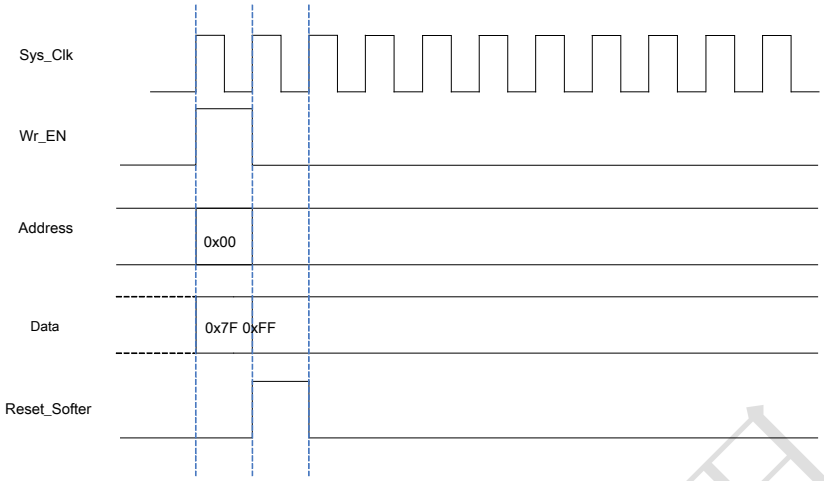


Fig 4.3 Chip software reset timing diagram

4.2 Chip power supply

HR_C6000 need 3.3V Power supply, built-in DCDC Module output 1.2V Used by digital and analog cores. Separate simulation by external circuit 3.3V ,digital 3.3V And simulation 1.2V ,digital 1.2V power supply. digital 1.2V And numbers 3.3V

Power supply shares digital ground; all analog 3.3V Common ground; all simulations 1.2V Common ground.

The power supply network is shown in the figure, where VCC33 Provide total power to the system, AVDD33 Simulate for the chip 3.3V power supply, DVDD33 Chip number 3.3V power supply. AVDD33 Provide chip built-in DCDC Module, needed to convert the output chip 1.2V Analog power AVDD12 And digital power DVDD12 .

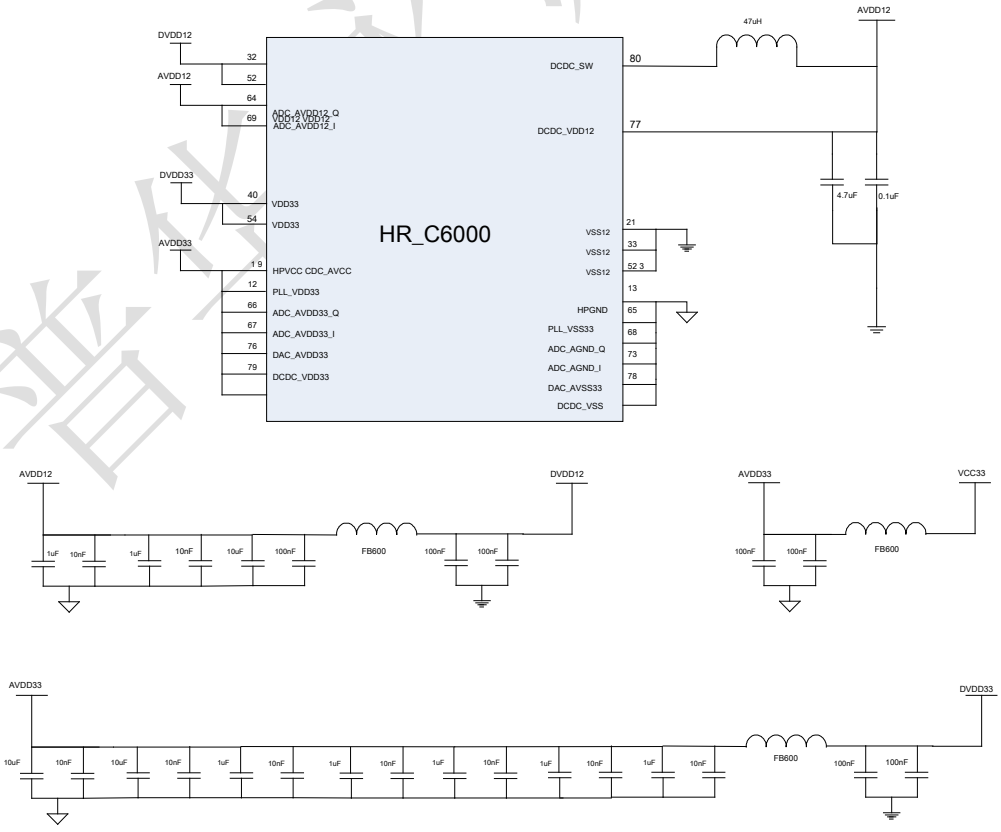


Fig 4.4 HR_C6000 Power reference circuit

4.3 Chip working clock block diagram and description

4.3.1 Clock circuit

HR_C6000 Requirements for crystal The best bias is 1.5V . Under this bias, the crystal output requirements Vpp≥2V . Chip clock by XTALI Pin input.

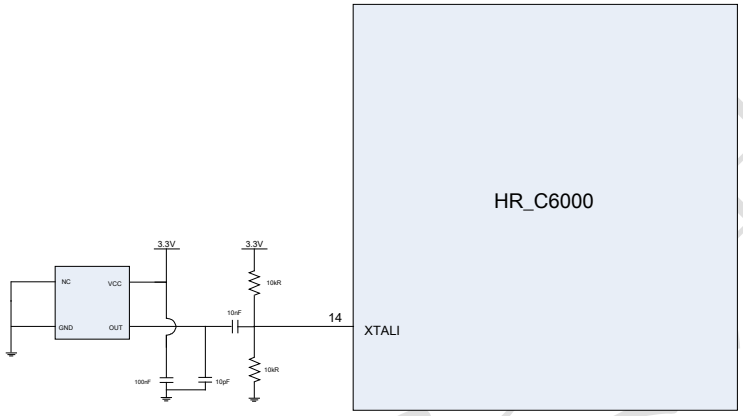


Fig 4.5 HR_C6000 Clock reference circuit

4.3.2 Clock configuration

Built-in configuration chip PLL Relevant registers of the PLL Lock to CLK , (Recommended value is 49.152MHz) , And the partial frequency in the chip is Sys_clk , Clk_codec , CLKOUT Three clocks, among them, Sys_clk Clock for system operation, through configuration register 0xB9 get, Sys_clk for 9.8304MHz ; Clk_codec Built into the chip Codec Working clock, by register 0xBA Configured, the frequency is 12.288MHz ;and CLKOUT Can be external Codec Or vocoder provides working clock, the clock frequency can be passed 0xBB Register to configure, additionally configure the register 0x0A of bit0 (ClkOut_enb) , You can control whether to output CLKOUT Clock, valid clock output when high level.

HR_C6000 At power-on, the internal working clock is directly provided by the external crystal oscillator at this time, that is 0x0A of bit7 for 1 , Change configuration reg0x0B with reg0x0C Then you need to wait for greater than 500μs ,wait PLL After the output is stable enough, the internal clock can be switched back from the crystal oscillator PLL Output.

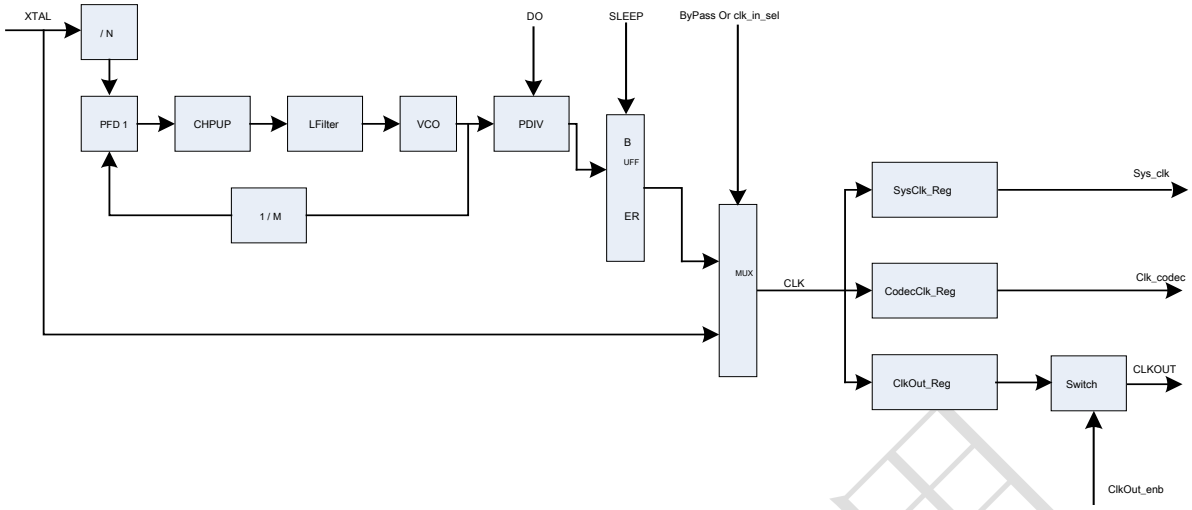


Fig 4.6 Chip working clock block diagram

Built-in chip PLL by 0x0B , 0x0C Register configuration, the specific calculation formula is as follows:

CLK = XTALI × PLLM / PLLN / NO ; among them:

- NO = 2 PLLDO
- 1M < XTAL / PLLN < 25MHz ;
- 200MHz < CLK × NO < 1000MHz ;
- PLLM> 1 ; PLLN> 1 ;
- will 0x0C Registered bit7 Configured as 1 , Can be PLL bypass ,at this time, PLL The output is CLK = XTALI ;
- will 0x0C of bit6 Configured as 1 Or chip PWD Raise the foot PLL Enter the sleep state PLL

  No clock output.
- Register 0x0A of bit7 (Clk_in_sel) Configured as 1 ,at this time CLK Do not choose PLL Output clock, but directly select XTALI , which is CLK = XTALI . table 4.1 Recommendation two Typical PLL Output clock configuration parameters

XTALI	PLL Configuration parameter	PLL Output clock	System clock configuration parameter	System output clock
12.288M	Reg0x0B = 0x40 Reg0x0C = 0x32	49.152M	Reg0xB9 = 0x05 Reg0xBA = 0x04 Reg0xBB = 0x02	Sys_clk = 9.8304 Clk_codec = 12.288M CLKOUT = 24.576M
29.4912 M	Reg0x0B = 0x28 Reg0x0C = 0x33	49.152M	Reg0xB9 = 0x05 Reg0xBA = 0x04 Reg0xBB = 0x02	Sys_clk = 9.8304 Clk_codec = 12.288M CLKOUT = 24.576M

4.4 Chip parameter configuration interface

MCU by U_SPI Mouth-pair HR_C6000 Perform parameter configuration, status control information, and write / read of send and receive data, and according to HR_C6000 Given TIME_SLOT_INTER , SYS_INTER , RF_TX_INTER , RF_RX_INTER Interrupt the corresponding interrupt processing. MCU Can also be passed GPIO Pin control chip Sleep status. The interface is shown below.

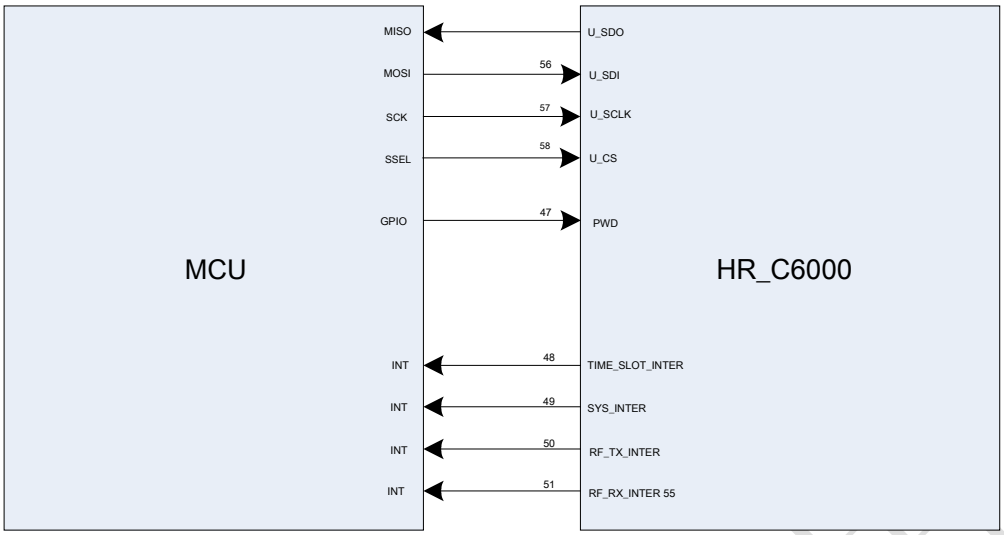


Fig 4.7 MCU versus HR_C6000 interface

Chip U_SPI The interface works at Slave Mode, interface timing is shown in the figure below.

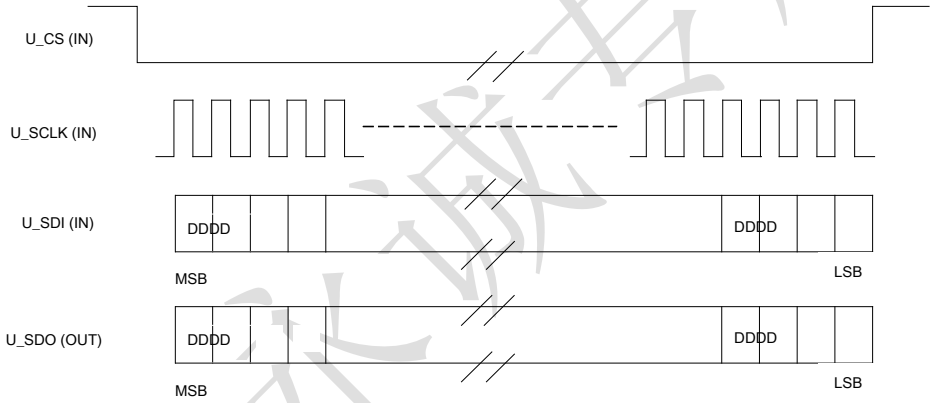


Fig 4.8 U_SPI Interface read and write timing

among them SCLK Maximum support 4M Clock rate.

MCU able to pass GPIO Pin control HR_C6000 of Sleep Status when GPIO When pulled high, the chip is in Sleep status, HR_C6000 All internal clocks are turned off. when GPIO When pulled down again, the chip is in normal working mode ByPass internal PLL , Through the crystal XTALI direct HR_C6000 Provide clock, wait 500μs Switch to internal after above PLL provide to HR_C6000 Working clock. as the picture shows, XTALI Input the clock signal for the crystal oscillator, PWD for HR_C6000 of Sleep signal, Sys_clk for HR_C6000 Working clock PLL_Sys_clk for PLL After output HR_C6000 The working clock requires a divided clock.

MCU Configuration PWD Is high, PWD in 100ns After stable and effective, at this time HR_C6000 All internal clocks are cleared, PWD After pulling it low again, the operating clock needs to be switched to XTALI ,wait PLL Stable output after frequency division PLL_Sys_clk After that, switch to PLL The output clock of the frequency division, the stability time is greater than 500μs .

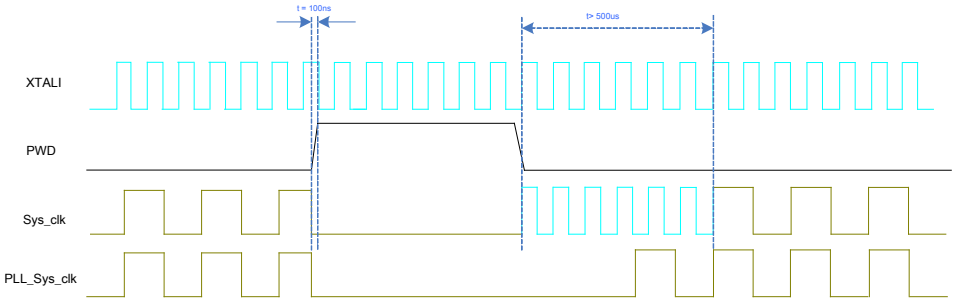


Fig 4.9 PWD Schematic diagram of control timing and working clock switching requirements

HR_C6000 provide 4 Interrupt pins, the interrupt low pulse is effective, the pulse width is 3 System clock (Sys_clk , 9.8304MHz) , SYS_INTER In order to obtain the system interruption of receiving and sending information, the sending process and receiving process prompt MCU Status or control information; TIME_SLOT_INTER for 30ms Time slot interruption, the interruption is at HR_C6000 After the establishment of the synchronization time slot has been generated cyclically, used for MCU establish one TDMA Time slot structure; RF_TX_INTER with RF_RX_INTER Interruption of radio frequency transceiver switching control is only generated in the process of time slot transceiver switching, which is convenient MCU Perform accurate and timely control of radio frequency channels, including RF_TX_INTER with RF_RX_INTER according to 30ms Generated alternately for the cycle. In order to facilitate the early start of radio frequency transmission control, you can set the register Reg0x12 control RF_TX_INTER And register Reg0xC0 control RF_RX_INTER relatively 30ms Border advance 0-6ms Can be configured.

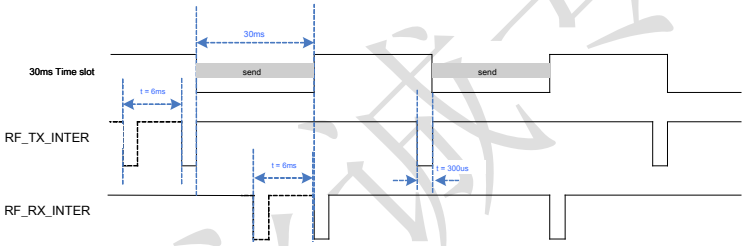


Fig 4.10 RF_TX_INTER with RF_RX_INTER Generate schematic

table 4.2 RF_TX_INTER Interrupt control register address description

address	Features
0x12	Bit [5: 0] Configure RF transceiver switch interrupt RF_TX_INTER relatively 30ms The advance of the boundary, the increment step is 100μs .
0xC0	Bit [5: 0] Configure RF transceiver switch interrupt RF_RX_INTER relatively 30ms The advance of the boundary, the increment step is 100μs .

4.5 Codec usage of

HR_C6000 Built-in CodeC ,achieve Mic Enter and LINEOUT Output, provide Mic Gain control and LINEOUT Volume control, effectively reduce user peripheral devices; at the same time for external CodeC Configuration standard I^2S Interface, users can also choose the appropriate one according to their needs Codec .

4.5.1 Use built-in Codec

Use built-in Codec The interface circuit is as follows. among them LINEOUT An audio amplifier is required for the port to drive the speaker.

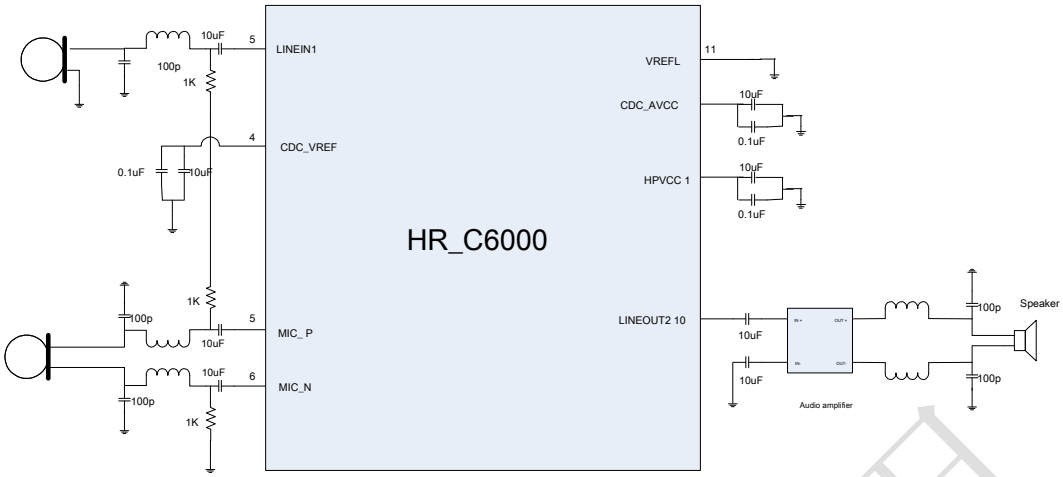


Fig 4.11 Use built-in Codec Interface circuit

Built-in Codec of ADC Duan He DAC There are multiple levels of gain adjustable at the end, picture 4.12 Built-in Codec Internal structure block diagram. The gains of each level are:

MIC_VOL , Adjust to enter ADC The previous analog input is adjustable 0 ,- 6 ,- 12dB Total 3 files;

ADLIN_VOL , Adjust to enter ADC The previous analog input is adjustable 0 ~ + 36dB , The step is 3dB ;

DALIN_VOL , Adjust the built-in Codec of DAC The gain size of the output data, the gain control step is 1.5dB can

In order to control whether the sound debugging becomes larger or smaller; when the adjustment becomes smaller, 0 Is the minimum; 0 The sound adjustment is invalid, and the sound size remains unchanged;

HPOUT_VOL , Adjust the built-in Codec of DAC Output data gain size, adjustable 0 , 2 , 4 , 6dB Of 4 files.

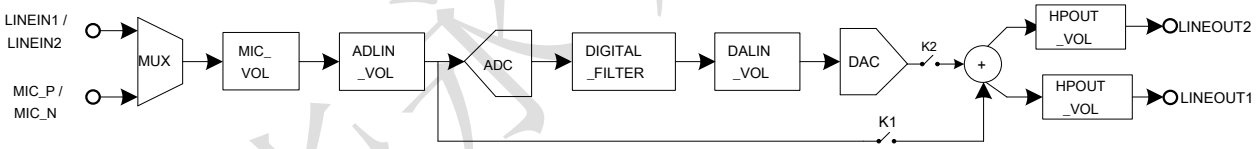


Fig 4.12 Built-in codec Internal structure diagram

All levels of gain can be configured through registers Codec The related registers are as follows. table 4.3 Built-in Codec Register address table

address	Features
0xE0	MCU control Codec Enable, and Codec of LINEIN end, MIC Duan He LINEOUT Enable
0xE2	Codec of DAC or ADC Switch on the Codec of Powerdown Control is enabled.
0xE3	K1 Switch control
0xE4	Bit7-6 : LINEOUT Gain control Bit5-4 : Mic The first stage gain; Bit3-0 : Mic Gain of the second stage.
0x3 7	DALIN_VOL Gain control, Bit5-0 The step size is 1.5dB Among them all 0 For the lowest sound, Bit6 Control the sound to become louder or smaller, Bit7 The sound adjustment is enabled for 0 At this time, the sound adjustment is invalid, and the sound size is unchanged.

4.5.2 Use external Codec

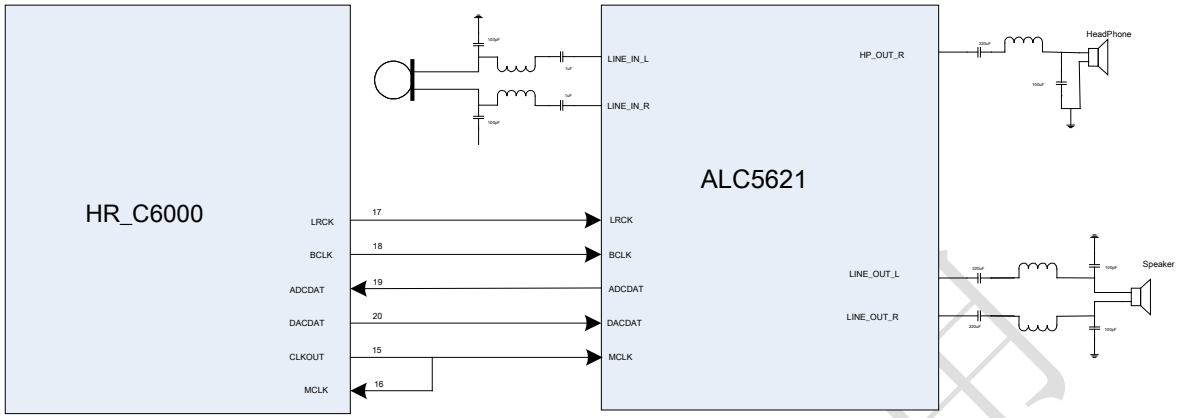


Fig 4.13 Use external Codec Interface circuit

when HR_C6000 Use external Codec When I 2 S Interface with Codec Perform data exchange. The interface timing is shown below.

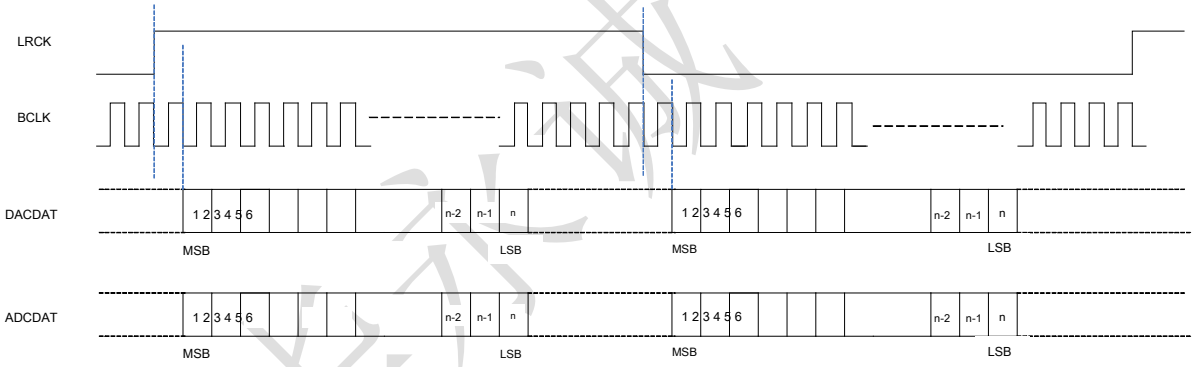


Fig 4.14 I 2 S Interface timing

Among them: 1, LRCK Clock frequency Codec Clock frequency and registers 0x32 , 0x33 Decide. By default LRCK clock

The frequency is 8KHz .

LRCK Clock frequency = Codec Clock frequency/[2*(Parameter value + 1)] , Where the parameter value is determined by {register 0x32 Value, register 0x33 Value} get. 2, BCLK Clock frequency Codec Clock frequency and registers 0x30 , 0x31 Decide.

BCLK Clock frequency = Codec Clock frequency/[2*(Parameter value + 1)] , Where the parameter value is determined by {register 0x30 Value, register 0x31 Value} get. 3. If using the default external Codec (ALC5621) ,then LRCK for 8KHz , BCLK for 512KHz . At the same time

Chip CLKOUT Pins and chips MCLK Pins are connected, CLKOUT Output 24.576MHz Clock, used inside the chip I2S work. Chip CLKOUT Pin with Codec The working clock input pin is connected. Built in chip Codec Chip CLKOUT Pins and chips MCLK The pins do not need to be connected.

All pins of the external Codec can be multiplexed as digital IO output, which can be used to control the high and low switching of the radio frequency and the main control chip. The high and low switching time can be any configuration with reference to the delay of the 30ms slot boundary or within 6ms in advance, the minimum configuration

The length is 100us.

Table 4.4

address	Features
0xC7 / C8	control LRCK Pin reuse, where C7 of Bit7 To enable multiplexing control, Bit6 Confirm high level relative 30ms The time slot boundary is advanced or delayed, 0 In advance, 1 Deferred Bit5-0 Control the amount of advance or delay in steps of 100us . among them C8 of Bit6 Confirm low level relative 30ms The time slot boundary is advanced or delayed, 0 In advance, 1 Deferred Bit5-0 Control the amount of advance or delay in steps of 100us
0xC9 / CA	control ADCDAT Pin reuse. Definition and LRCK The multiplexing method is the same.
0xCB / CC	control MCLK Pin reuse. Definition and LRCK The multiplexing method is the same.
0xCD / CE	control BCLK Pin reuse. Definition and LRCK The multiplexing method is the same.
0xCF / D0	control DACDAT Pin reuse. Definition and LRCK The multiplexing method is the same.

As shown below, to LRCK Pin control is used as an example to illustrate the schematic diagram of high and low level control. The other pin control methods are the same as this.

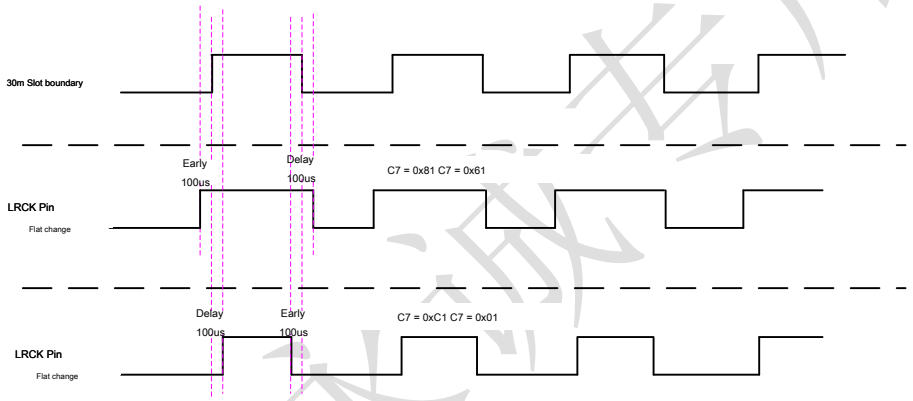


Fig 4.15 LRCK Pin reuse for general purpose IO Control interface timing

4.6 Vocoder

HR_C6000 Can be used McBSP with CHS Seamless serial interface AMBE3000 with AMBE1000 Waiting for the vocoder chip, while providing standards SPI with I 2 S Interface with Hongrui HR_V3000 Vocoder, Tsinghua University SELP Vocoder, 712 plant AVDS The vocoder is seamlessly connected, supports encrypted voice and data interfaces, and provides interfaces for digital voice recording, playback, and prompt input.

4.6.1 Hongrui HR_V3000 Vocoder interface definition

HR_V3000 versus HR_C6000 by V_SPI Transmit the compressed and encoded digital voice stream or the digital voice stream to be decoded, pass I 2 S Interface and vocoder transmission PCM Data, where HR_C6000 of I 2 S The interface works in the main mode; MCU by UART Interface with HR_V3000 Pass the voice encryption and decryption key or voice frame synchronization information. V_SPI The interface timing of the port is shown in the figure below.

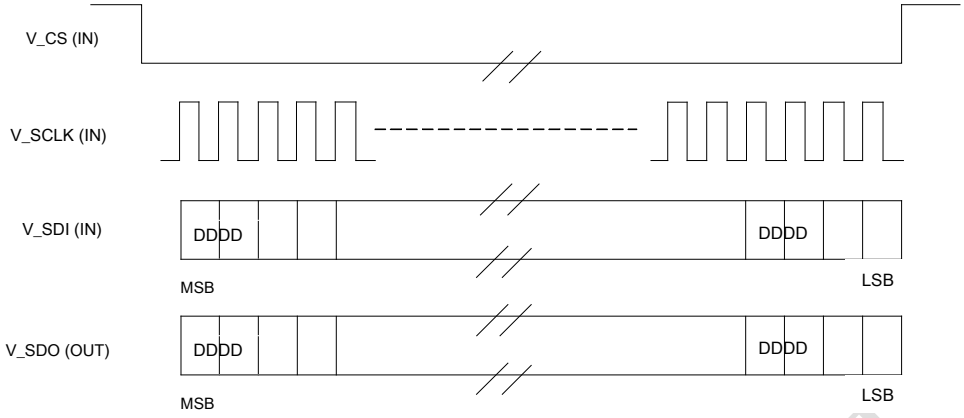


Fig 4.16 General V_SPI Interface read (write) timing

among them SCLK Maximum support 4M Clock rate.

V_SPI The frame format is shown below. What needs to be explained is:

- V_SPI The interface can only perform one operation at a time, read or write.
- When reading, Cmd = 0x83 , Addr = 0x00 ,read 27 Pc Data (byte) . When writing, Cmd = 0x03 , Addr = 0x00 ,write 27 Pc Data (byte) .

Cmd	Addr	Data0	Data1 …	Datan

Fig 4.17 V_SPI Frame format

by V_SPI interface HR_C6000 Hongrui HR_V3000 Vocoder communication, only need to HR_C6000 Register reg0x06 Configured as 0x24 . HR_V3000 versus HR_C6000 as well as MCU The connection block diagram is shown in the figure.

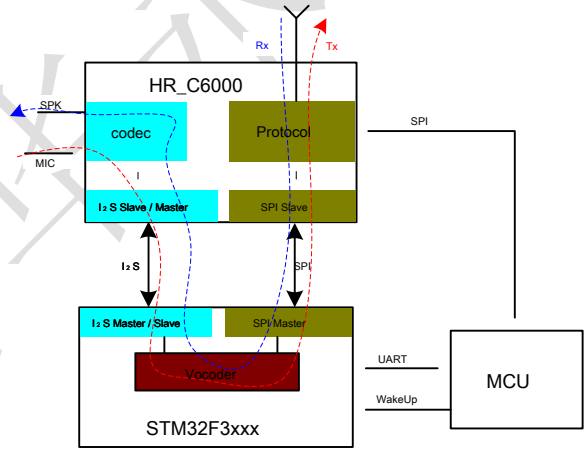


Fig 4.18 HR_V3000 Vocoder and HR_C6000 Connection diagram

As shown 4.19 for I2S Interface timing.

I2S Working in main mode, need to pass the register 0x2F Configuration I2S_CK_M Clock frequency, calculated as codec working frequency/(2*(register 0x2F Value + 1)) . Pass register 0x32 , 0x33 Configuration I2S_FS_M Clock frequency (configured I2S_FS_M The clock frequency must be 8KHz), The calculation method is codec working frequency/(2*({ register 0x32 value, 0x33 Value} + 1)) . Simultaneously I2S_CK_M Frequency> 34 * I2S_FS_M Frequency, and codec Clock frequency> = 6 * I2S_CK_M frequency.

when I2S When working in the main mode, through the register 0x36 [6] , You can close I2S_CK_M , I2S_FS_M signal. when 0x36 [6] = 0 , Turn on the two signals, otherwise turn off the two signals.

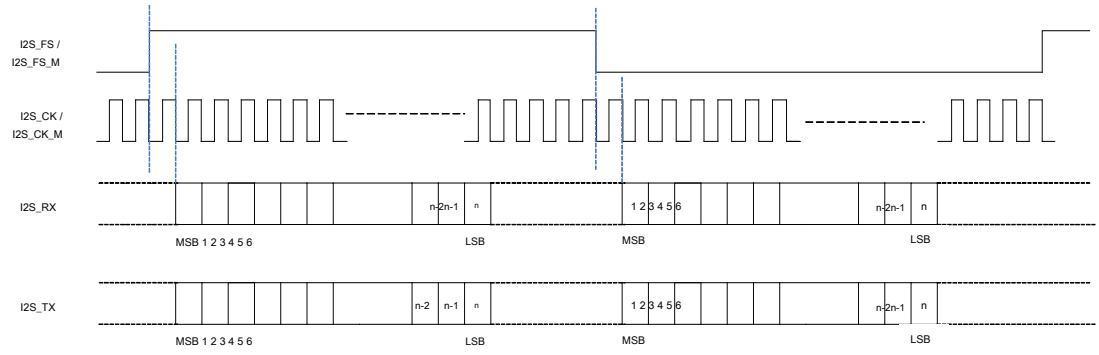


Fig 4.19 I 2 S Interface timing

HR_V3000 For detailed instructions on the use of vocoders, please refer to " HR_V3000 Vocoder instructions. doc ".

4.7 Launch module

HR_C6000 Built-in two high-performance DAC , With single-ended output, supports baseband IQ , Intermediate frequency and two-point modulation and other RF interfaces, the amplitude and offset of the two signals are adjustable.

The user can select the corresponding transmit interface through the configuration register, the two output signal offsets and the two output signal amplitudes.

In addition, in order to control the power consumption of the chip, the user can set 0x25 Register in DAC Turn it off when not working. Configuration 0x25 of Bit3 , Bit2 Can choose HR_C6000 According to the transmission time slot DAC Control, or by MCU By configuration Bit5 , Bit4 Correct DAC To control the working status of table 4.5HR_C6000 Baseband transmit control register address

address	Features
0x01	Bit7 select HR_C6000 Correspondence between the transmission port and the RF transmission port; Bit [5: 4] Choose to configure one of the four transmission modes. among them 2'b00 Means to send IF mode, 2'b10 Send baseband IQ mode, 2'b11 Means sending two-point modulation mode.
0x02	Baseband transmission output I Offset value of the road.
0x04	Baseband transmission output Q Offset value of the road.
0x07	IF frequency word height 8bit
0x08	IF frequency word 8bit
0x09	IF frequency word low 8bit
0x12	Bit7 Configure smoothing enable; bit6 Configure two-point modulation test square wave output enable; bit [5: 0] The amount of radio frequency interruption advance, the increment step is about 100μ s.
0x25	DAC Work control word.
0x2E	Send advance configuration value, due to the different delay of the RF channel, in order to ensure the air DMR The signal strictly corresponds to sending at the time slot boundary, the configuration of this register can offset this delay, the step is 100μs . The fixed delay of the internal channel is 400μs , So when there is no delay on the RF side, this register should be configured as 0x04 .
0x45	Adjust two-point modulation MOD2 (DAC_IVOUT) Amplitude
0x46	Adjust two-point modulation MOD1 (DAC_QVOUT) Amplitude
0x47	Define two-point modulation offset adjustment value, total 10bit , Which is high 2bit Defined in

	reg0x48 Low 2bit in.
0x48	Bit [1: 0] Define two-point modulation offset adjustment value, total 10bit , Of which low 8bit Defined in reg0x47 in

4.7.1 Baseband IQ modulation

By setting the register 0x01 [5: 4] = 2'b10 ,Make HR_C6000 Work on sending baseband IQ Mode can be configured by 0x02 , 0x04 Register adjustment IQ The offset values of the two signals.

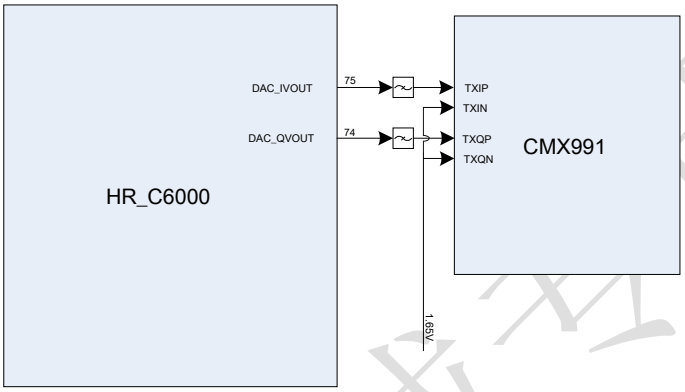


Fig 4.20 Baseband IQ Modulation interface circuit

As shown in FIG, HR_C6000 Baseband IQ The signal is a single-ended output, and the signal bias voltage is 1.65V ,Baseband IQ The signal is connected to the filter CMX991 of TXIP , TXQP ,and CMX991 The negative end of the baseband signal TXIN , TXQN Then pick 1.65V DC voltage. The filter is used to filter the baseband transmitted signal DAC The converted image signal.

Baseband IQ In mode, the maximum differential output amplitude when sending random signals is 2725mV . By setting the register 0x02 Adjustable output I Road offset, the adjustment range is about ± 264mV , The minimum adjustment step is 3.3mV .

By setting the register 0x04 Adjustable output Q Road offset, the adjustment range is about ± 264mV , The minimum adjustment step is 3.3mV .

By setting the register 0x12 [7] , You can choose to send a gentle starting point, if configured 0x12 [7] = 1'b0 , The starting point of the gentle rise is 1.65V , If configured 0x12 [7] = 1'b1 , The starting point of the gentle rise is 0V .

By setting the register 0x12 [5: 0] , You can configure the RF control interrupt RF_TX_INTER relatively 30ms Slot boundary advancement, adjustable range is 0μs ~ 6300μs , The minimum adjustment step is 100μs .

By setting the register 0x45 [3: 0] The output can be adjusted simultaneously IQ Two-way amplitude, adjustable range is about 170mV ~ 2725mV , The minimum adjustment step is 170mV .

4.7.2 Two-point modulation

By setting the register 0x01 [5: 4] = 2'b11 ,Make HR_C6000 Work in two-point modulation mode, can be configured 0x02 , 0x04 The registers adjust the offset value of the two-point modulation signal respectively. As shown in the figure below, the two-point modulation signal is adjusted by two op amps to adjust its signal offset and signal amplitude MOD1 , MOD2 Two signals control the crystal and VCO , To achieve two-point modulation, where Bias1 versus Bias2 The bias voltages of the op amps can be passed DAC Or the digitally adjusted resistance, AD5165 It is the op amp feedback resistor, which can be used to adjust the signal amplitude.

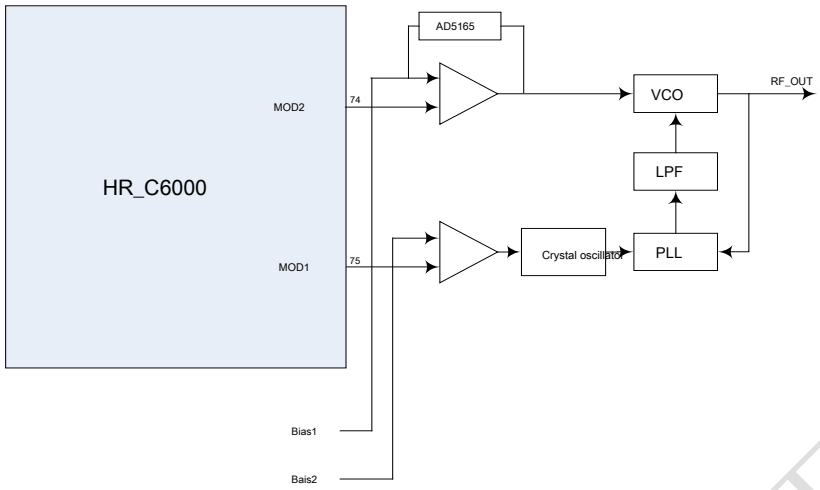


Fig 4.21 Two-point modulation interface signal

In two-point modulation mode, the maximum differential output amplitude when sending random signals is approximately 2240mV . Through configuration registers 0x01 [7] Can adjust the modulation frequency offset mapping relationship, configuration 0x01 [7] = 0 , The relationship between the corresponding symbol and the modulation frequency deviation is:

table 4.6 Correspondence between signal symbol and modulation frequency deviation

symbol	Modulation frequency deviation
+ 3	1944 Hz
+ 1	648 Hz
- 1	-648 Hz
-3	-1944 Hz

Configuration 0x01 [7] = 1 , The relationship between the corresponding symbol and the modulation frequency deviation is:

table 4.7 The sign of the signal corresponds to the modulation frequency deviation system

symbol	Modulation frequency deviation
+ 3	-1944 Hz
+ 1	-648 Hz
- 1	648 Hz
-3	1944 Hz

By setting the register 0x04 Adjustable output MOD1 Road offset, the adjustment range is about ± 422mV , The minimum adjustment step is 3.3mV .

By setting the register 0x02 Adjustable output MOD2 Road offset, the adjustment range is about ± 422mV , The minimum adjustment step is 3.3mV .

By setting the register 0x12 [7] , Can choose to send a gentle rise starting point, configuration 0x12 [7] = 1'b0 , The starting point of the gentle rise is 1.65V , If configured 0x12 [7] = 1'b1 , The starting point of the gentle rise is 0V .

By setting the register 0x12 [6] = 1'b1 , You can send 40Hz Square wave, used for two-point modulation debugging. By setting the register 0x12 [5: 0] , You can configure the RF control interrupt RF_TX_INTER relatively 30ms Slot boundary advancement, adjustable range is 0μs ~ 6300μs , The minimum adjustment step is 100μs .

By setting the register 0x46 Adjustable output MOD1 Road amplitude, adjustable range is about 8.75mV ~ 2240mV , The minimum adjustment step is 8.75mV .

By setting the register 0x45 Adjustable output MOD2 Road amplitude, adjustable range is about 8.75mV ~ 2240mV , The minimum adjustment step is 8.75mV .

When sending using two-point debugging mode, if receiving RF channel needs HR_C6000 Output DC voltage for control

Crystal oscillator voltage, you need to configure 0x25 Registered Bit5 = 1 and Bit3 = 0 To make that way DAC It is normally open. At this time, you can configure the register 0x47 [1: 0] with 0x48 [7: 0] (among them 0x47 [1: 0] High 2bit), Set MOD1 The output voltage value in the receiving state, the adjustment range is 0 ~ 3.3V .

4.7.3 IF IQ modulation

Set up 0x01 [5: 4] = 2'b01 , HR_C6000 Working at mid-frequency IQ mode. HR_C6000 Interface with RF and baseband IQ similar. In this working mode, the intermediate frequency can be passed 0x07 , 0x08 , 0x09 Three registers are obtained, and the calculation formula is shown below.

IF frequency word IF_word = {0x07 , 0x08 , 0x09} ;

IF_word = IF_Feq / Sys_clk × $2^{twenty\ four}$. among them, IF_Feq Is the required IF frequency; Sys_clk System clock for chip 9.8304MHz .

4.7.4 IF modulation

Set up 0x01 [5: 4] = 2'b00 , HR_C6000 Work in IF mode. HR_C6000 IF output mode and IF IQ The main difference is that the IF IQ After the two signals are combined, they are output at the single-ended interface. Intermediate frequency word definition method and intermediate frequency IQ The pattern is the same.

4.8 Receive module

HR_C6000 Built-in two high-performance ADC , Support baseband IQ IF IQ , Intermediate frequency and other RF interfaces, and support two channels with adjustable amplitude and offset.

Control two channels through register configuration ADC The voltage at full-scale input of the signal. In addition, in order to control the power consumption of the chip, you can choose MCU According to the receiving time slot, the corresponding ADC Set to sleep mode in the transmission slot, or by MCU Control accordingly ADC Working status. table 4.8 HR_C6000 Baseband transmit control register address

address	Features
0xA1	Bit7 select AF Receiving mode or non AF Receive mode, if you select non AF Receive mode, pass 0x01 of Bit [3: 2] Select one of multiple reception modes.
0x01	Bit6 select HR_C6000 Correspondence between receiving port and radio frequency receiving port; Bit [3: 2] Choose to configure one of the three receive modes. among them 2'b00 Indicates receiving IF mode, 2'b01 Indicates receiving intermediate frequency IQ mode, 2'b10 Receiving baseband IQ mode.
0x03	Baseband receive input I Offset value of the road.
0x05	Baseband receive input Q Offset value of the road.
0x07	IF frequency word height 8bit
0x08	IF frequency word 8bit
0x09	IF frequency word low 8bit
0x12	Bit7 Configure smoothing enable; bit6 Configure two-point modulation test square wave output enable; bit [5: 0] The amount of radio frequency interruption advance, the increment step is about 100μ s.
0x26	ADC Work control word.

0x27	ADC Work control word.
0x28	ADC Work control word.
Schedule 0x52	Configure high signal energy detection threshold 8 Bits of information.
Schedule 0x53	Low signal energy detection threshold 8 Bits of information.
Schedule 0x54	Configure timing synchronization module detection threshold
Schedule 0x55	Configure the detection threshold of the detection module

4.8.1 Baseband IQ

By setting 0x01 [3: 2] = 2'b10 So that HR_C6000 Work on baseband IQ Mode, by configuration 0x03 , 0x05 The register can be used for receiving IQ The offset of the signal is adjusted. Where the register 0x03 Adjustable AD Input I Road offset, the adjustment range on the digital side is- 127 ~ 127 ,register 0x05 Adjustable AD Input Q Road offset, the adjustment range at the digital end is -127 ~ 127 .

In addition, set the schedule register 0x52 , 0x53 , You can set the threshold of signal energy detection, where 0x52 High configuration 8 Bit information, set the schedule register 0x54 , Can set the detection threshold of the timing synchronization module, set the schedule register 0x55 , The detection threshold of the detection module can be set.

Use baseband IQ The receiving block diagram is shown below.

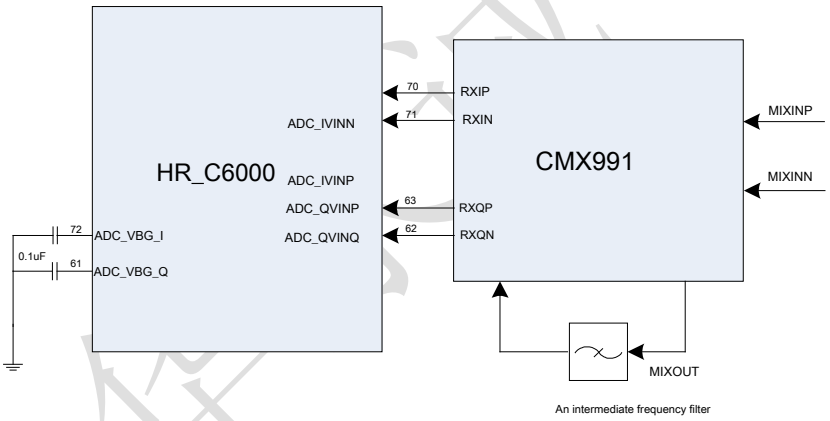


Fig 4.22 Baseband IQ Receive reference interface circuit

To HR_C6000 versus CMX991 Connection as an example, the received RF signal is filtered and amplified to enter CMX991 At the receiving end, via 991 Internally mixed to 45MHz (or 90MHz) Output after an intermediate frequency, after being amplified by an intermediate frequency filter, it is sent back 991, Perform the second mixing to the baseband and send the baseband differential signal to HR_C6000 . One of the IF filters is mainly used to filter adjacent channel interference signals.

4.8.2 IF mode

By setting 0x01 [3: 2] = 2'b00 So that HR_C6000 Working in IF mode, through configuration 0x03 , 0x05 The register can adjust the offset of the received intermediate frequency signal, and can be configured by 0x07 , 0x08 , 0x09 Correct HR_C6000 Set the received IF frequency, see the calculation formula 4.7.3 . By setting the schedule register 0x52 , 0x53 , You can set the threshold of signal energy detection, where 0x52 High configuration 8 Bit information; set the schedule register 0x54 , Can set the detection threshold of the timing synchronization module, set the schedule register 0x55 , Can set the detection threshold of the detection module.

The reception block diagram using IF mode is shown below.

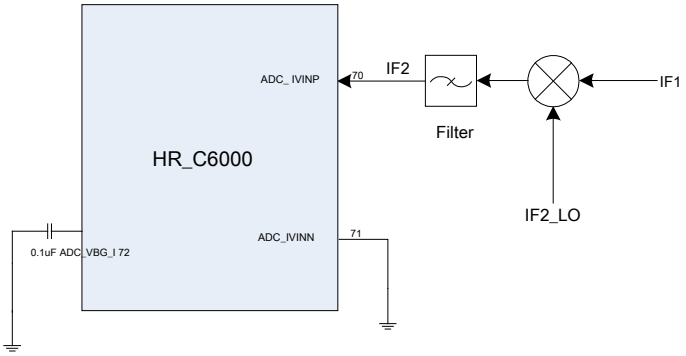


Fig 4.23 IF receiving reference interface circuit

The received signal is filtered, amplified, mixed to low intermediate frequency, and sent to the low intermediate frequency amplifier HR_C6000 of AD Pin ADC_IVINP ,and ADC Negative side ADC_IVINN It can be grounded or receive the bias voltage of the intermediate frequency signal. It should be noted that the low-IF filter is mainly used to filter adjacent channel interference signals, when the channel interval is 25KHz , The filter bandwidth

Optional ± 7.5KHz , When the channel interval is 12.5KHz , The filter bandwidth is selectable ± 3.75KHz Or ± 4.5KHz .

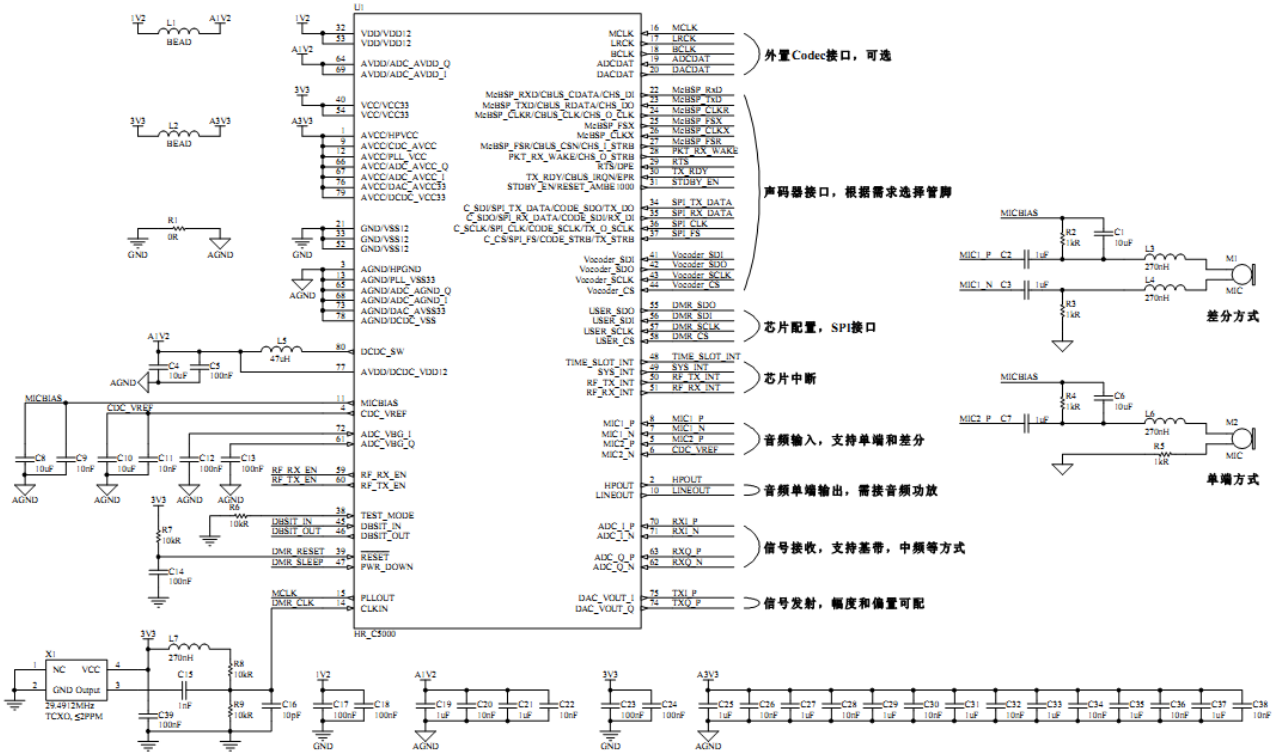


Fig 4.24 HR_C6000 Reference interface circuit

5 Layered function description

HR_C6000 Using a flexible layered design model, according to different user needs, flexible and open different layers for users to use.

The layered design uses a three-layer architecture, as shown in the figure.

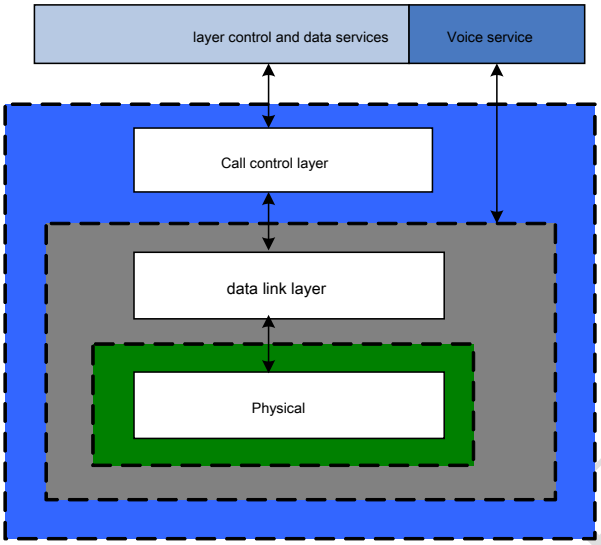


Fig 5.1 HR_C6000 Three-tier open architecture

The one-layer mode mainly solves the channel filtering of the baseband or low-IF signal and the modulation and demodulation process of the signal, as defined in the green dotted frame in the above figure. The user needs to solve the channel coding and decoding and the processing of all communication protocol stacks by using the one-layer mode, which has the greatest development flexibility and development workload.

The two-layer mode is mainly based on the opening of all the contents of one layer, and completes the work of channel coding and decoding, interleaving, deinterleaving, and verification, as defined in the gray dashed box in the above figure. The user only needs to solve the processing flow of the communication protocol stack, which has greater development flexibility and a moderate development workload.

The three-tier model refers to HR_C6000 according to DMR All application functions defined by the protocol complete the modulation and demodulation, coding and decoding of the signal, and the protocol stack design of all standardized application functions, as defined in the blue dotted frame in the above figure. Users use these application functions, only need to configure the corresponding function register, you can quickly and easily use all DMR Protocol customized voice and data services.

HR_C6000 Mainly based on the two-layer mode development, users do not need to pay attention to channel coding and decoding interleaving and the underlying modulation and demodulation process.

5.1 Interrupt instructions

5.1.1 Interrupt usage description

The corresponding interrupt of the three-layer function is sys_inter , The interrupt consists of two sub-interrupts, after receiving the interrupt, MCU Read interrupt status register 0x82 , You can go through the register 0x81 Mask the corresponding interrupts and pass the register at the same time 0x83 Clear the interrupt signal list of the corresponding bit to obtain 8 Types of interrupts, including:

Bit7 : DMR In mode: indicates that the request to send is rejected

This interrupt has no substatus register. in DMR In the mode, it indicates that the sending request is rejected because the channel is busy;

Bit6 : DMR In mode: indicates the start of sending; in MSK In mode: indicates that the ping-pong buffer half full interrupt is sent

in DMR In mode, there is a sub-status register at the beginning of transmission 0x84 ,able to pass 0x85 Mask the corresponding interrupt. The sub-status register indicates 7 This generates an interrupt to start transmission, including:

Bit7 : Start voice transmission

Bit6 : OACSU Request to send interrupts, including the first send and retransmit requests.

Bit5 : End-to-end voice enhanced encryption interrupt, including EMB72bits Update interruption and voice 216bits Key Update interrupt, through register 0x88 of Bit5 ~ Bit4 To distinguish, where 01 Express EMB72bits Update interrupted, 10 Voice 216bits Key update interrupted.

Bit4 : Vocoder Configuration return interrupt (this interrupt is MCU Manual configuration AMBE3000 When HR_C6000 to MCU Send configuration complete interrupt). **This interrupt is only used when external AMBE3000 The use of vocoder is effective.**

Bit3 : Data transmission starts

Bit2 : Partial data retransmission

Bit1 : All data retransmitted

Bit0 : The vocoder initialization interrupt is completed. **This interrupt is only used when external AMBE3000 or AMBE1000 The use of vocoder is effective.**

in MSK In mode, there is no sub-interrupt status.

Bit5 : DMR In mode: indicates the end of sending; MSK In mode: indicates that the end of transmission is interrupted.

in DMR In mode, there is a sub-status register at the end of transmission 0x86 ,able to pass 0x87 Mask the corresponding interrupt. The sub-status register indicates 6 This generates an interrupt that ends the transmission, including:

Bit7 : Indicates that the service sending is completely over, including voice and data. MCU Distinguish this sent Whether it is voice or data. Confirming the completion of the data service refers to receiving the correct feedback Response package.

Bit6 : Represents a sliding window data service that does not require immediate feedback Fragment Length confirmation packet Sending is complete.

Bit5 :voice OACSU Wait timeout

Bit4 : Interrupt processing in Layer 2 mode, MCU Dispatch the configuration information to the chip for the last processing timing control interrupt, If after this interruption, MCU If all the information about the next frame to be sent has not been written to the chip, the next time slot cannot be configured as a transmission time slot. This interrupt is only valid when the chip is operating in Layer 2 mode.

Bit3 : Indicates the one that needs feedback Fragment Confirm that the data packet is sent. This interrupt is mainly used for After the confirmation SMS has sent all the data packets or the data packets that need feedback in the sliding window data service are sent, it will be notified MCU Start waiting Response Package timer.

Bit2 : ShortLC Receive interrupt

Bit1 : BS Activation timeout interrupt

Bit0 :no. in MSK In mode, there is no substate interrupt.

Bit4 : DMR In mode: indicates that the rear access is interrupted; MSK In mode: indicates that the response is interrupted

DMR In the mode, the post-access interrupt has no sub-status register. After receiving the interrupt, it indicates that the voice communication mode of access is the post-access mode. in MSK In mode, this interrupt has no substatus register.

Bit3 : DMR In mode: indicates that the analysis of the control frame is interrupted; MSK In mode: indicates receiving interrupt.

in DMR In mode, this interrupt has no sub-status register, but the right and wrong of its received data and the type of reception are 0x51 Register given, use DLLRecvDataType , DLLRecvCRC Explain the type of data received and the situation of right and wrong, MCU According to the corresponding status display, you can also mask the corresponding interrupt. in MSK Mode, this interrupt has no substate interrupt.

F Framed EMB The information analysis completion prompt is also the completion of the interruption, by judging 0x51 register SyncClass = 0 Make a distinction.

Bit2 : DMR In mode: indicates that service data reception is interrupted; FM In mode: means FM Function detection interrupted.

in DMR In mode, the interrupt has a sub-status register 0x90 , The substatus register has 3 Types:

1. 0x80 Indicates that the entire information reception verification passed, and after the business data verification passed, MCU by SPI Port extraction RX end 1.2KRAM Middle address 0x30 After the data, the length of the data is defined by the corresponding field of the received frame header;
2. 0x00 Indicates that the entire information reception verification
3. 0x40 Indicates that an abnormal interruption of a non-confirmed SMS occurred; FM In mode, the interrupt has a sub-status register 0x90 , The substatus register has 1 Types:

1. 0x10 Express FM Function detection interrupt matching, in FM In mode, the corresponding interruption of the receiving interruption is detected and the corresponding analog sound output is turned on.

Bit1 : DMR In mode: indicates that the voice exits abnormally;

in DMR Mode, DMR The reason for the abnormality in the mode is the unexpected abnormal voice interrupt generated inside the state machine, through the register address 0x98 of Bit2 ~ Bit0 Obtain the corresponding voice anomaly type.

Bit0 : The physical layer works alone to receive interrupts

The physical layer works alone to receive an interrupt without a sub-status register. The interrupt is generated in the physical layer's separate working mode. The interrupt is generated after receiving data, and the notification MCU Read the corresponding register to get the received data. This interrupt is generally used in the physical layer mode to test the bit error rate or other performance.

The processing method of the system interrupt is as follows. The specific response tree is as follows (not included FM mode):

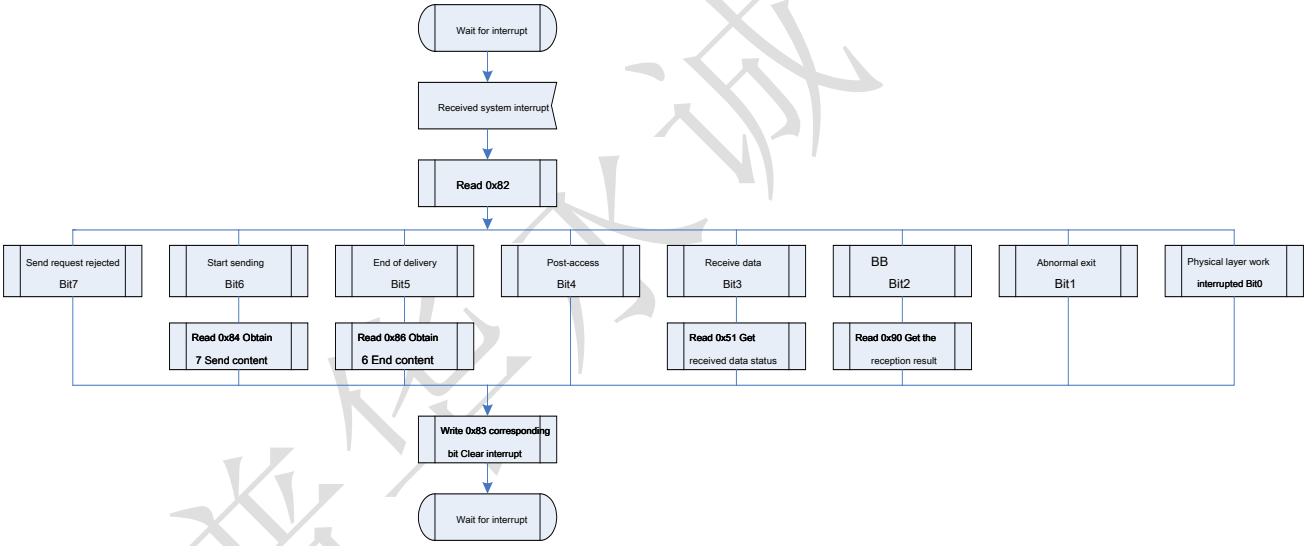


Fig 5.2 Interrupt response tree

Time_slot_inte Interrupt is TDMA Time slot interruption, when HR_C6000 After the synchronization slot of 30ms

The interval is given continuously. Until synchronization is lost.

5.2 Interface reading and writing instructions

Users U_SPI The content of the visit includes the register system parameter table, register appendix, TX end 1.2KRAM

with RX end 1.2KRAM , The access frame format is:

Cmd	Addr	Data0	Data1 ...	Datan

Fig 5.3 U_SPI Access frame format

table 5.1 Cmd Express SPI The reading and writing status of the port and the corresponding Address space

Cmd	W IsRead			Bit7	1 Indicates that this operation is read, 0 Indicates that this operation is writing
		Read and write initial address extension		Bit6	0 Does not expand, 1 Expand
				Bit5-Bit3 Keep	
		OPMode		Bit2-Bit0	000 Keep 001 Represents the operation auxiliary parameter configuration table, 010 Indicates the origin of the operation RAM , Read and receive end RAM , 100 Indicates the operating system parameter table, 101 Indicates configuration AMBE3000 register 110 Represents the write end of the operation RAM , Read end RAM , 111 Indicates configuration AMBE1000 register

Cmd The highest bit selects whether this time is a read operation or a write operation, low 3bit Select the category of this read and write operation.

Addr This is the starting address for reading and writing. The data written (or read) in the future will start from this starting address and accumulate one by one. CS When valid, it will continue to accumulate.

- when Cmd [6] = 1'b0 , Addr Express 8bits (High order first), the read and write start address is Addr ;
- when Cmd [6] = 1'b1 , Addr Express 16bits (High order first), the read and write start address is { Addr [2: 0], Addr [15: 8]} .

1, Registration of register system parameter table Device 0x01 Write 0x80 The format is:

Cmd	Addr	Data
8'b 0 0000 100	8'b0000 0001	8'b1000 0000

2, Read end 1.2KRAM From 0x30 Started 2 Byte data (data content is in order 0x0 1 , 0x02) The format is:

Cmd	Addr	Data0	Data1
8'b 1 0000 010	8'b0011 0000	8'b0000 0001	8'b0000 0010

In addition, Cmd of OPMode Bit is 101 , 111 Different 2 Class external vocoder register configuration, 011

To read and write the start-up sound or other prompt sounds.

5.3 HR_C6000 RAM Assignment definition

table 5.2 Under the second layer working mode TX end 1.2KRAM The space allocation defines the

frame type	address	Explanation
voice LC Header	0x00 ~ 0x0b	0x00 ~ 0x08 :total 72bit For control letter; 0x09 ~ 0x0b :total 24bit For verification information, MCU Optional.
voice PI Header	0x00 ~ 0x0b	0x00 ~ 0x09 :total 80bit For control information; 0x0a ~ 0x0b :total 16bit For verification information, MCU Optional.
voice EMB	0x00 ~ 0x09	0x00 ~ 0x08 :total 72bit For control letter; 0x09 : bit7-bit3 total 5bit For verification information, MCU Optional. The information here is about to prepare to send voice A Prepare at the same time.

voice A	0x30 ~ 0x4a	total 216bit For voice frame information.
voice B	0x30 ~ 0x4a	total 216bit For voice frame information.
voice C	0x30 ~ 0x4a	total 216bit For voice frame information.
voice D	0x30 ~ 0x4a	total 216bit For voice frame information.
voice E	0x30 ~ 0x4a	total 216bit For voice frame information.
voice F	0x30 ~ 0x4a	total 216bit For voice frame information.
RC frame	0x00 ~ 0x01	0x00 , 0x01 of bit7-bit5 ,total 11bit information
voice Terminator	0x00 ~ 0x0b	0x00 ~ 0x08 :total 72bit For control letter; 0x09 ~ 0x0b :total 24bit For verification information, MCU Optional.
CSBK	0x00 ~ 0x0b	0x00 ~ 0x09 :total 80bit For control information; 0x0a ~ 0x0b :total 16bit For verification information, MCU Optional.
MBC Header	0x00 ~ 0x0b	0x00 ~ 0x09 :total 80bit For control information; 0x0a ~ 0x0b :total 16bit For verification information, MCU Optional.
MBC Intermedia	0x00 ~ 0x0b	0x00 ~ 0x0b :total 96bit For control information;
MBC Last	0x00 ~ 0x0b	0x00 ~ 0x0b :total 96bit For control information;
DataHeader	0x00 ~ 0x0b	0x00 ~ 0x09 :total 80bit For control information; 0x0a ~ 0x0b :total 16bit For verification information, MCU Optional.
DataRate1_2	0x00 ~ 0x0b	0x00 ~ 0x0b :total 96bit Data information;
DataRate3_4	0x00 ~ 0x11	0x00 ~ 0x0b :total 144bit Data information;
DataRate1	0x00 ~ 0x17	0x00 ~ 0x0b :total 192bit Data information;
Idle	0x18 ~ 0x23	0x18 ~ 0x23 :total 96bit For control information;
Short LC	0x24 ~ 0x28	0x24 ~ 0x26 , 0x27 of bit7-bit4 :total 28bit Control information 0x28 :total 8bit Verify the information.
voice F frame EMB	0x29 ~ 0x2C	voice F Frame fill information or 0x29 Store super frame number (KeyID), 0x2A high 3bit Store Encrypted serial number (ALOG ID)
Data control frame EMB RC	0x4b ~ 0x50	Data control frame embedded 48bit of RC Information or 0x4b , 0x4c height of 11bit of RC Encoder input
C_RC frame(PDT) 0x00 ~ 0x0a		0x00 , 0x01 of bit7-bit5 :total 11bit RC information; 0x02 ~ 0x08 :total 56 bit Control information 0x09 ~ 0x0a :total 16 bit Verification information
196 information	0x30 ~ 0x48	196bit Control information
Test send	0x00 ~ 0x48	Send mode test to store data address
FM Data address 1	0x030 ~ 0x22f	total 512bytes Data information. Can be written externally FM send

		Voice data can also be sent internally from Codec Voice data
FM Data address 2	0x230 ~ 0x42f	total 512bytes Data information. Can be written externally FM send Voice data can also be sent internally from Codec Voice data
Encrypted key stream data storage Store	0x495 ~ 0x4af	total 216bit , 27 bytes

table 5.3 Under the second layer working mode RX end 1.2KRAM The space allocation defines the

frame type	address	Explanation
voice LC Header	0x00 ~ 0x0b	0x00 ~ 0x08 :total 72bit For control letter; 0x09 ~ 0x0b :total 24bit For verification information.
voice PI Header	0x00 ~ 0x0b	0x00 ~ 0x09 :total 80bit For control information; 0x0a ~ 0x0b :total 16bit For verification information.
voice EMB	0x00 ~ 0x09	0x00 ~ 0x08 :total 72bit For control letter; 0x09 : bit7-bit3 total 5bit For verification information.
RC frame		RC Decoding result 11bit Information is saved in registers
voice Terminator	0x00 ~ 0x0b	0x00 ~ 0x08 :total 72bit For control letter; 0x09 ~ 0x0b :total 24bit For verification information.
CSBK	0x00 ~ 0x0b	0x00 ~ 0x09 :total 80bit For control information; 0x0a ~ 0x0b :total 16bit For verification information.
MBC Header	0x00 ~ 0x0b	0x00 ~ 0x09 :total 80bit For control information; 0x0a ~ 0x0b :total 16bit For verification information.
MBC Intermedia	0x00 ~ 0x0b	0x00 ~ 0x0b :total 96bit For control information;
MBC Last	0x00 ~ 0x0b	0x00 ~ 0x0b :total 96bit For control information;
DataHeader	0x00 ~ 0x0b	0x00 ~ 0x09 :total 80bit For control information; 0x0a ~ 0x0b :total 16bit For verification information.
DataRate1_2	0x00 ~ 0x0b	0x00 ~ 0x0b :total 96bit Data information;
DataRate3_4	0x00 ~ 0x11	0x00 ~ 0x0b :total 144bit Data information;
DataRate1	0x00 ~ 0x17	0x00 ~ 0x0b :total 192bit Data information;
Idle	0x00 ~ 0x0b	0x00 ~ 0x0b :total 96bit For control information;
C_RC frame(PDT) 0x00 ~ 0x08		0x00 ~ 0x06 :total 56 bit Control information 0x07 ~ 0x08 :total 16 bit Verification information RC Decoding result 11bit The information is saved in registers.
EMB_48_INFO_0	0x1F ~ 0x24	Time slot 0 Received 48bitEMB Area information
EMB_48_INFO_1	0x25 ~ 0x2a	Time slot 1 Received 48bitEMB Area information
ShortLC	0x2b ~ 0x2f	Receiving end CACH Field 36bit ShortLC Data, where 0x2F of

		low 4bit Useless data
264bit_info_0	0x30 ~ 0x50	Current time slot 0 Analysis results 264bit Information, including speech frames 216bit information
264bit_info_1	0x60 ~ 0x80	Current time slot 1 Analysis results 264bit Information, including speech frames 216bit information
264bit_soft_0	0xa8 ~ 0x1af	Current time slot 0 Analysis results 264 Soft information, every byte bit5-bit0 .
264bit_soft_1	0x1c8 ~ 0x2cf	Current time slot 1 Analysis results 264 Soft information, every byte bit5-bit0 .
FM Data address 1	0x030 ~ 0x22f	total 512bytes Data information.
FM Data address 2	0x230 ~ 0x42f	total 512bytes Data information.
Decrypt key stream data storage Store	0x495 ~ 0x4af	total 216bit , 27 bytes

5.4 Support frame type

5.4.1 Time slot framing

Slot framing, there are 3 Modes: voice time slot packet, data time slot packet and RC package.

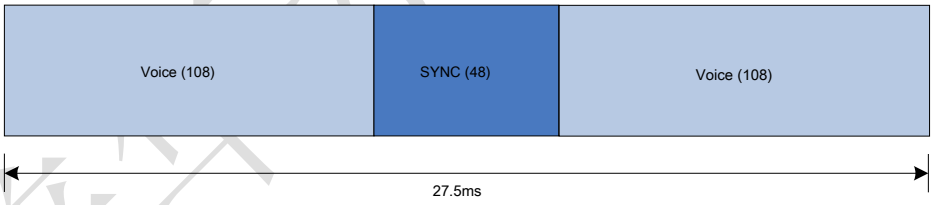


Fig 5.3 Voice time slot packet with synchronization header

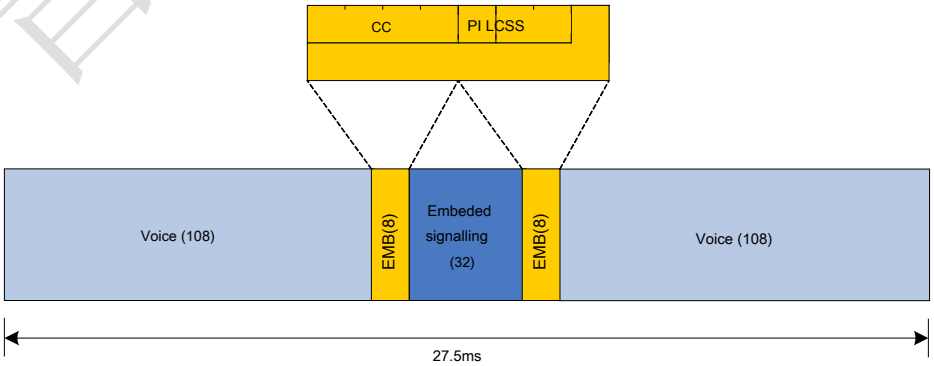


Fig 5.4 Voice time slot EMB data

1 , Support six kinds of voice time slot packet framing, and according to the superframe rule, determine the use of synchronization header in the voice frame or LC or Null ,

Formed according to standards A (SYNC) , B (LC) , C (LC) , D (LC) , E (LC) , F (Null) Superframe. Details include:

a) Support the opt-in of sync header;

b) stand by EMB 7bit Join, yes EMB get on QR (16,7,6) coding;

c) stand by LC 72bit Join, join 5bit CS Code, variable length BPTC Encode, interleave, and add

Into 4 In time slots (128bit) ;

table 5.3 Group call 72bit LC Information Sheet

Information element	Length	Remark
Protect Flag (PF)	1	
Reserved	1	This bit shall be set to 0
Full Link Control Opcode (FLCO)	6	Shall be set to 000000
Feature set ID (FID)	8	Shall be set to 00000000
Service Option	8	
Group address	twenty four	
Source address	twenty four	

table 5.4 Call 72bit LC Information Sheet

Information element	Length	Remark
Protect Flag (PF)	1	
Reserved	1	This bit shall be set to 0
Full Link Control Opcode (FLCO)	6	Shall be set to 000011
Feature set ID (FID)	8	Shall be set to 00000000
Service Option	8	
Group address	twenty four	
Source address	twenty four	

d) stand by Null Time slot join;

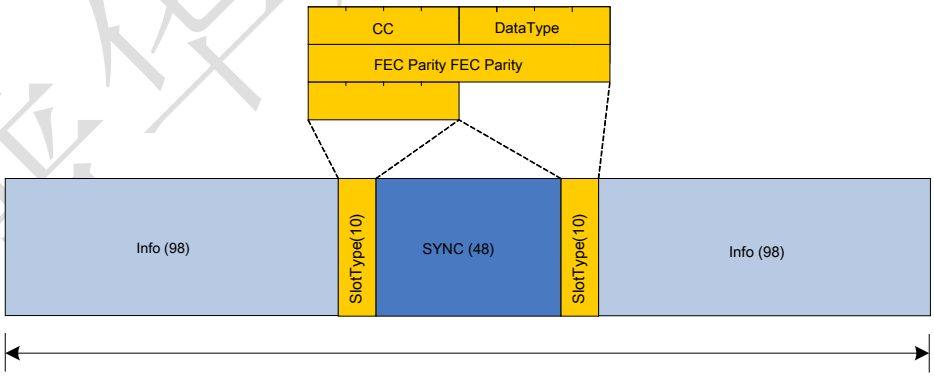


Fig 5.5 Structure chart of data and control frame

2 , stand by LC package

a) Support to join 72bit LC , CRC24bit Verify and join CRC Mask (Header with Terminator the difference),

get on BPTC (196 , 96) Encoding, forming voice Head frame;

b) Support 72bitLC Information formation ShortLC Package for embedding into speech EMB region;

c) stand by LC Package dynamic update;

3 , stand by CSBK package, MBC Packages and data packages; detailed internals include:

a) Support to join Slot Type (20bit) ,include CC , DataType ,get on Golay (20 , 8) coding;

b) stand by SYNC Join

c) Support to join 80bit CSBK , CRC16bit Verify and join CRC Mask, proceed BPTC (196 , 96)

Coding, interweaving;

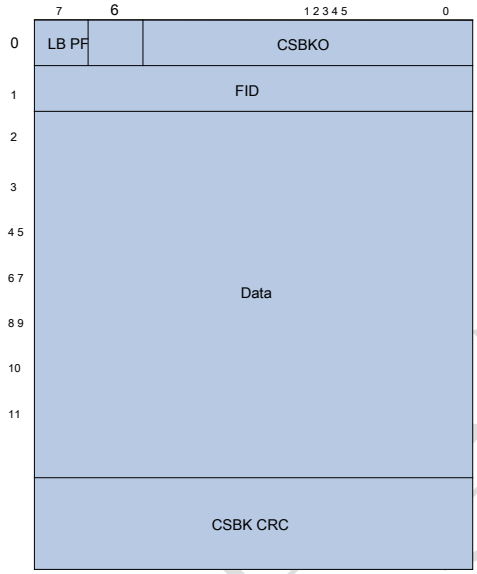


Fig 5.6 CSBK 80bit information chart

d) Support to join 96bit Idle ,get on BPTC (196 , 96) Coding, interweaving;

e) Support to join 80bit MBC header , CRC16bit Verify, join CRC Mask, proceed BPTC (196 ,

96) Coding, interweaving;

f) Support to join 96bit MBC Data BPTC (196 , 96) Coding, interweaving;

g) Support to join 80bitMBC lastBlock ,get on CRC16bit Verify BPTC (196 , 96) coding,

Intertwined

h) Support data packet header, join 80bit Data CRC16bit Verify, join CRC Mask, proceed

BPTC (196 , 96) Coding, interweaving;

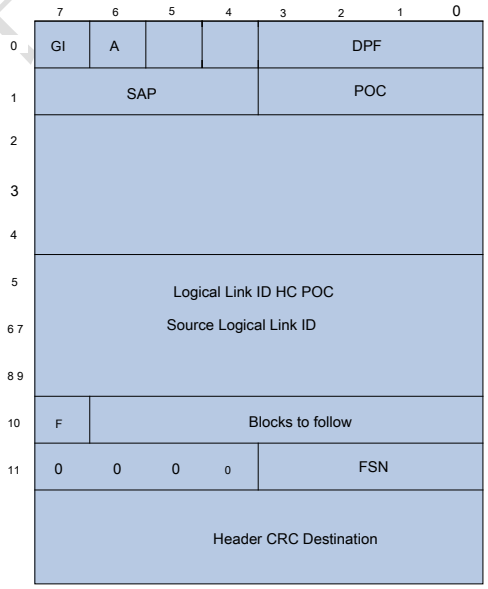


Fig 5.7 Unacknowledged packet header

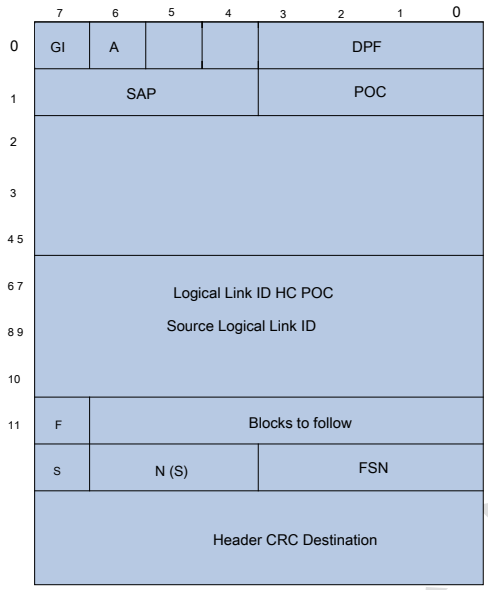


Fig 5.8 Confirm the packet header

i) Support rapid generation according to application requirements Unconfirmed data header , Confirmed data header ,

Response data header , Proprietary data header , Status / Precoded short data header ,

Raw short data header , Defined short data header with Unified Data transport data header ;

j) stand by Rate 1/2 The data format of the model, added 96bit Data BPTC (196 , 96) Coding, delivery

Weave

k) stand by Rate 1/2 The last time slot data of the mode is added 64bit Data 32bitCRC Check (check

Contains all data), proceed BPTC (196 , 96) Coding, interweaving;

l) stand by Rate 3/4 The data format of the model, added 96bit Data Trellis Coding, interweaving;

m) stand by Rate 3/4 The last time slot data of the mode is added 64bit Data 32bitCRC Calibration (calibration

Test contains all data), proceed Trellis Coding, interweaving;

n) stand by Rate 1 The data format of the model, added 96bit data;

o) stand by Rate 1 The last time slot data of the mode is added 64bit Data 32bitCRC Checksum

All data included);

p) stand by 3 Rate-based confirmed Data transfer, join 7bit SN ,get on 9bitCRC Check, add mask

Codes (different rates, different masks), encode and interleave at different rates, add data 32bitCRC ;

q) Support feedback packet data slot, join 1 - 2 Data feedback package 32bitCRC Verify, enter

Row BPTC (196 , 96) Coding, interweaving;

r) stand by UDT of last Block , To the data 16bitCRC Verify BPTC (196 , 96) coding,

Intertwined

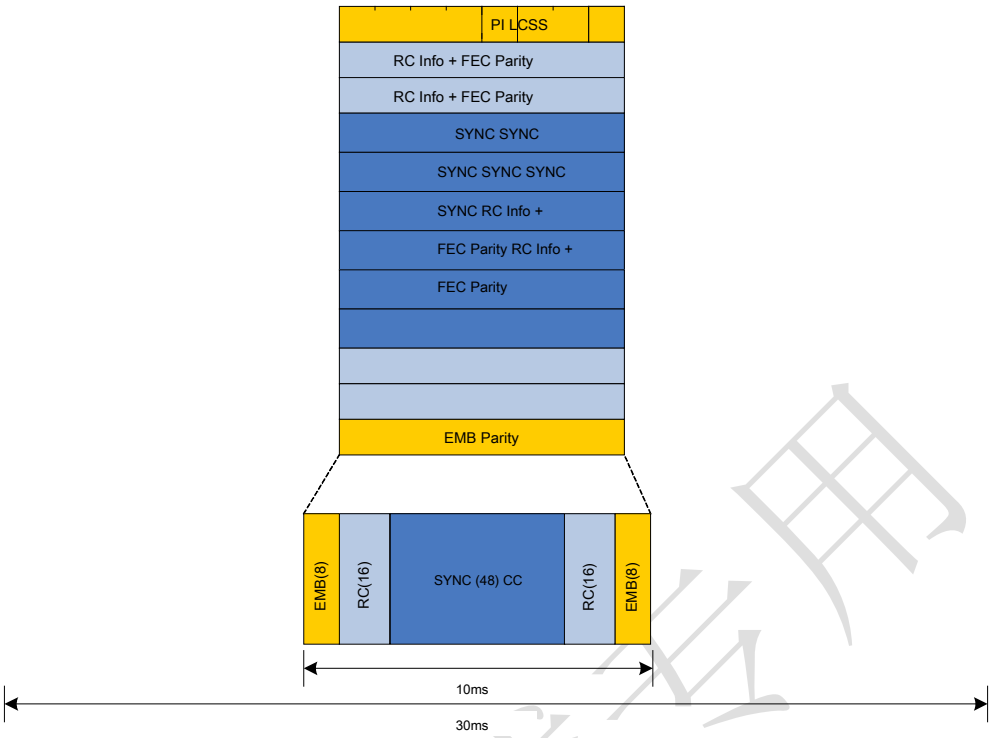


Fig 5.9 independent RC Frame structure

4 , Support time slot RC with EMB of RC signal;

a) Support to join 7bitEMB ,get on QR (16,7,6) coding;

b) Support to join 11bit RC Signal, variable length BPTC ,Correct 32bit Interweave and add to RC unit;

5 , Receive according to SYNC Determine the content type of the frame, according to Slot Type , FLCO , CSBKO , LB , DPF

Determine the type of the received frame, and then perform deinterleaving, decoding, and verification corresponding to the transmission according to the received frame type.

5.4.2 Framing mode

Continuous mode :

1) Support voice superframe framing, can be set LC Header , PI Header Or only PI Header Mode, end since Dynamically form a superframe and join LC Terminator ;

2) Support data 4.8kbps Framing, adding data LC Header , Data and LC Terminator ;

3) Support data 9.6kbps Framing, adding data LC Header , Data and LC Terminator ;

Time slot mode:

1) Support voice superframe framing, can be set LC Header , PI Header Or only PI Header Mode, end since Dynamically form a superframe and join LC Terminator ;

2) Supports various data types 4.8kbps Framing, adding data LC Header , Data and LC Terminator ;

5.4.3 Frame definition and use

Configuration register reg0x10 for 0x68 , The system works in Layer 2 mode; configuration registers reg0x40 for 0x43 , reg0x41 for 0x40 By default, the system is configured in passive receiving state. Other configurations are sufficient by default.

Send frame type configuration reg0x50 Register designation.

table 5.5 Frame type coding corresponds to off Frame

type	LocalDataType	Whether voice
voice LC Header	0001	0
voice PI Header	0000	0
voice A	0000	1
voice B	0001	1
voice C	0010	1
voice D	0011	1
voice E	0100	1
voice F	0101	1
RC frame	0110	1
voice Terminator	0010	0
CSBK	0011	0
MBC Header	0100	0
MBC Intermedia	0101	0
MBC Last	0101	0
DataHeader	0110	0
DataRate1_2	0111	0
DataRate3_4	1000	0
DataRate1	1010	0
Idle	1001	0
Reserved	1011	0
Reserved	1100	0
Reserved	1011	0
Reserved	1110	0
Reserved	1111	0

To send data in Layer 2 mode, users need to prepare the content of the data frame to be sent in the next time slot according to the type of frame sent. If the frame type has been defined in the above table, the user can configure the register Reg40 of bit3 Make sure that users complete the verification process corresponding to these frame types or use HR_C6000 Automatically complete the frame check digit generation process. If by HR_C6000 Automatically completed, the check code generation process is strictly in accordance with DMR The agreement standard is generated;

MCU Check in HR_C6000 There is no need to care about the verification method and the content of the verification code, but to directly perform the next encoding process in accordance with the original data. For example, if the user needs to have MCU Complete one CSBK The verification process needs to be generated first 80bitCSBK Data information, and then generated according to the self-defined verification method 16bit The check digit of 96bit

Write information HR_C6000 Send RAM the address of 0- address 11 ,then HR_C6000 Take these data directly BPTC Encoding and subsequent framing process. If it is a user-defined frame type, you need to store the generated verification information bits in the sending end after the verification is completed RAM Space designated location, HR_C6000 The check information is used as a part of the transmission information bit to enter the subsequent encoding and framing process.

The schematic diagram of the sending process is shown in the figure below.

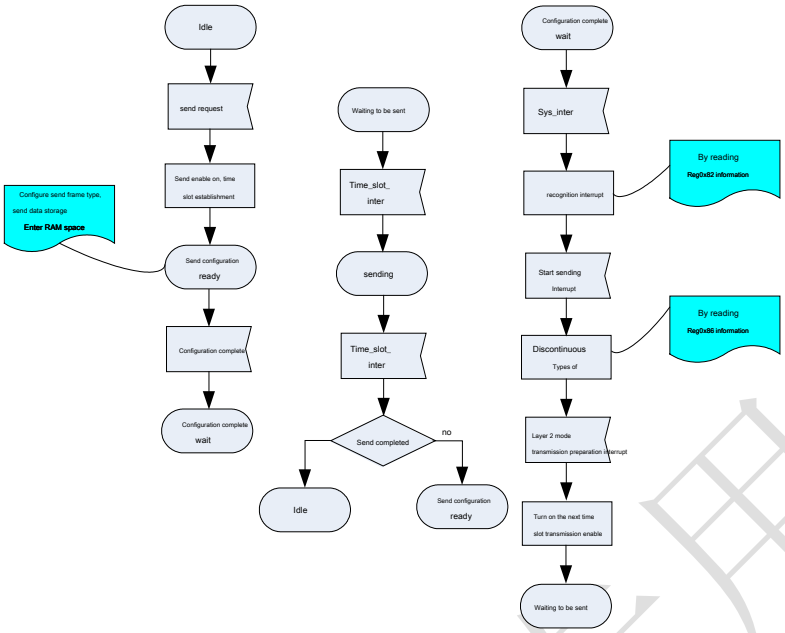


Fig 5.10 Flow chart of Layer 2 sending process

5.4.4 Description of working mode

Working in the second layer mode, what is needed in the whole machine 30ms The time-slot synchronization time axis consists of HR_C6000 Provide, while HR_C6000 provide 30ms There are two modes of timeline, one is by HR_C6000 Counting by own clock, stable supply 30ms Interrupt, called active mode, the other is HR_C6000 which provided 30ms Interruptions are constantly based on HR_C6000 Receive the signal (including the signal of the sync head) to adjust your own 30ms (Approximate) Interrupt output, called passive mode.

Active mode: CPU Set up HR_C6000 Active mode (register reg0x40 Bit5 Configured as 1 ,among them Bit6 , Bit7 There must be a 1) , Establish time slots, MCU provide 30ms Interrupt.

Passive mode: CPU Set up HR_C6000 register reg0x40 Bit5 Configured as 0 (among them Bit6 , Bit7 There must be a 1) , HR_C6000 Enter the receiving state The system starts to establish synchronization according to the synchronization information of the received signal, and continuously adjusts the synchronization time axis according to the received synchronization information, which is provided to MCU 30ms (Approximately) interrupted.

After establishing a complete timeline, the chip has the conditions for sending and receiving. On this basis, the chip will provide CPU Time slot interrupt Time_slot_inter , To inform CPU The middle of the time slot of the entire time axis, CPU According to the time axis to plan the corresponding receiving and sending, to carry out correct control and data transmission.

register 0x40 of Bit7 For sending, Bit6 For receiving, this is CPU Inform the chip of the control signals that can be sent or received. Only one of these two signals is valid, the time axis will be established, but these two signals will not independently control the transmission and reception of each time slot. register 0x41 of Bit7 (Send) and Bit6 (receive).

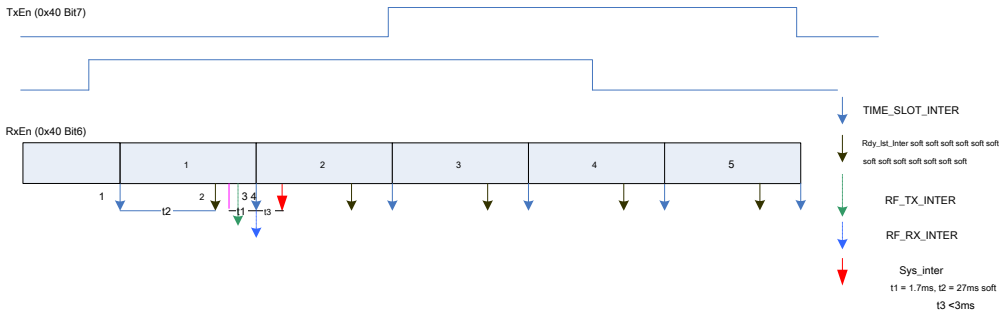


Fig 5.11 Schematic diagram of Layer 2 interrupt distribution

In Layer 2 mode, once the timeline is established (whether in passive or active mode), the chip will continue to 30ms

Give the period shown above TIME_SLOT_INTER with Rdy_Ist_inter . among them Rdy_Ist_inter Is not an independent interrupt pin, the terminal is Sys_inter Multiplexing an interrupt pin output, multiplexing mode and 5.1.1 The use of the three-layer interrupt in the description is the same.

among them t1 The time is the start time when the chip sends coded framing, t2 Prepare data for the software and configure the time for sending and receiving control commands, t3 For the end of the time slot until it can be sent Sys_inter Break to CPU time.

Chip in place 1 Or location 2 , Given TIME_SLOT_INTER or Rdy_Ist_Inter , CPU The time slot can be set according to one of these two interrupts 2 Will be sent or received (0x41 , Bit7 , Bit6).

Chip in place 3 , TIME_SLOT_INTER When the interrupt is given, CPU Can get the time slot 2 The sending and receiving status of (0x42 , Bit7 , Bit6).

If the time slot 1 Yes receive, then in the location 4 CPU The data received in this time slot can be read as CPU Provide the basis for decision-making.

Hypothetical time slot 1 For receiving and in position 1 (TIME_SLOT_INTER Break) to the location 2 (Rdy_Ist_inter Interrupt) Set the time slot before this period 2 To send, the chip will give RF_TX_INTER ,for CPU To set the relevant parameters of the RF channel.

Hypothetical time slot 1 For sending, and in place 1 (TIME_SLOT_INTER Break) to the location 2 (Rdy_Ist_inter Interrupt) Set the time slot before this period 2 To receive, the chip will give RF_RX_INTER ,for CPU To set the relevant parameters of the RF channel.

According to the active and passive modes established by the time axis, the whole machine's control of the transceiver mode of the time slot is combined into a working mode:

1) Actively send

Active sending means that the system is currently out of synchronization, initiates a call, and generates synchronization information locally. This situation is mainly used in HR_C6000 Actively initiate single and duplex transmission.

MCU Set send register 0x40 Turn on active sending 0xA3 ;

The establishment of this flag will cause the chip to actively send synchronization information, through TIME_SLOT_INTER to MCU send 30ms Interruption of intervals;

MCU Upon receipt 30ms After interruption, read 0x42 status bit7-5 , To judge the sending and receiving status of the current time slot:

001 Indicates that the current time slot is a working time slot, but the sending and receiving are completely closed;

101 Indicates that the current time slot is a working time slot and transmission is on;

011 Indicates that the current time slot is a working time slot, and reception is on;

xx0 Indicates that the current time slot is a non-working time slot, and there is no need to open the transceiver

MCU Obtained HR_C6000 To determine the working requirements of the next time slot according to the protocol. in 30ms After the synchronization time slot is established, if the next time slot needs to be sent, the t2 Internal writing requires framing (including 196bit rate 1 data flow, 144bit rate 3/4 data flow, 96bit rate 1/2 data flow, 96bit Custom control

Information frame, 80bit Data frame header or CSBK Data Frame, 72bit Voice frame header, frame end) data, data format and content requirements in accordance with DMR Protocol standards are designed and Rdy_Ist_inter When interrupted, set register 0x41 Value to determine whether to send the next time slot 0x80 (send), 0x00 (Do not send); if shielded Rdy_Ist_inter Interrupt, you can 30ms Interrupt (TIMER_SLOT_INTER , Location in the figure 1) Time to configure directly 0x41 Registers, that is, configure whether to send or not to send before data writing, so that the user must ensure that t2 Complete all data preparations requiring framing within the time.

Chip in t1 Time to start reading 0x40 of Bit7 Flag, if 1 , Then the data in the data cache will be t1 The map is sent within the time.

CPU Can be based on RF_Tx_Inter Interrupt the configuration of the relevant RF channel for sending.

2) Active reception (active full duplex)

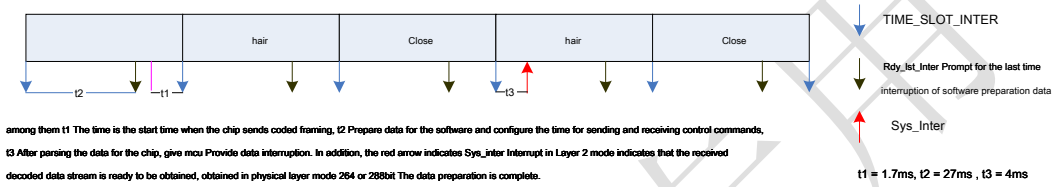


Fig 5.12 Schematic diagram of active full-duplex transceiver interrupt

Active reception occurs at the time of active full-duplex. Active full-duplex means that the call originator first sends a sending request. MCU Configuration register 0x40 After turning on the send enable, take the initiative to establish 30ms Interrupted. After the establishment of the synchronization time slot, MCU Configuration register 0x41 ,distribution HR_C6000 Transmit time slot and receive time slot, so as to achieve full-duplex communication.

Active sending and receiving, through control 0x41 of TxNxtSlotEn (Bit7)with RxNxtSlotEn (Bit6) Realize active full-duplex. The received synchronization time slot does not update the synchronization of the system.

Reception in this mode is called active reception.

3) Passive reception

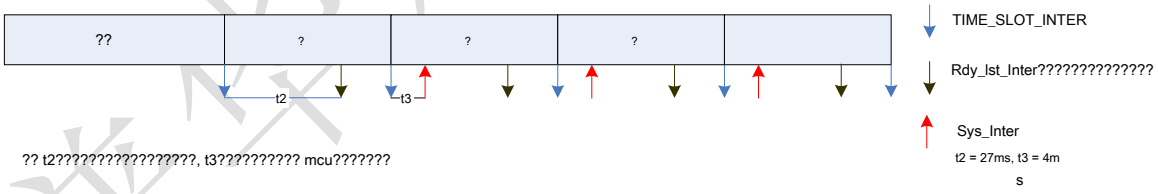


Fig 5.13 Schematic diagram of passive receiving interrupt

Passive reception means MS Synchronization information is obtained through reception, and the local synchronization information is updated using the reception. Mainly used in passive reception of single and duplex.

MCU Set the receive register to enable passive mode 0x40 Set as 0x43 ;

HR_C6000 Start receiving, but before receiving the receive interrupt, the received register 0x41 Need to be set to 0x40 , Enter the state of continuous reception (called blind reception). After receiving the reception interrupt, the internal synchronization mechanism of the chip will establish a synchronization mechanism consistent with the received signal. Therefore, it is recommended to judge whether to receive the next time slot according to the received data The way is to receive Sys_inter After interruption, read 0x52 of cc To determine whether the synchronization is established, if cc If it does not match, it is configured 0x41 for 0x20 Reacquire synchronization information, if cc Match, according to 0x51 The content of the register determines the transmission and reception of the next time slot. If the data is correct, the 0x41 Write 0x00 Turn off the reception, and then TIME_SLOT_INTER When the interrupt comes, start receiving, the chip will generate the corresponding RF_rx_inter Interrupt, use the interrupt to control the radio frequency module.

The synchronization mechanism in passive mode ensures that if there is synchronization information received and the gap with the existing local synchronization is within

1.25ms Within, then the real-time synchronization adjustment will be performed, if the reception synchronization disappears (the received signal disappears, does not control 0x41 (Receiving), the chip according to the existing local synchronization information 30ms Count and provide TIME_SLOT_INTER Interrupt until MCU shut down TxEn (0x40 Bit7)with RxEn (0x40 Bit6);at this time MCU Can be determined to be in a passive or active state based on actual conditions;

Parsing frame content of the current receiving time slot (including 196bit rate 1 data flow, 144bit rate 3/4 data flow, 96bit rate 1/2 data flow, 96bit Custom control information frame, 80bit Data frame header or CSBK Data Frame, 72bit (Speech frame header, frame end) will be in the next time slot t3 Given after time Sys_Inter Interrupt, MCU Can read frame type register according to interrupt 0x82 Determine the type of receive interrupt, 0x51 The register judges the received data frame type and check information, 0x52 Register judgment CC Match result, prompt MCU Can be from RX end RAM Spatially remove the corresponding deframe information.

4) Passive transmission (passive full duplex)

Passive mode also occurs at the moment of full duplex, in which case full duplex refers to MS The synchronization information is obtained through reception. The system establishes a synchronization time slot and performs full-duplex communication.

Passive full-duplex is MCU control 0x41 A combination of passive reception and passive transmission. The specific operation mode combines the same processing of passive receiving and passive sending modes.

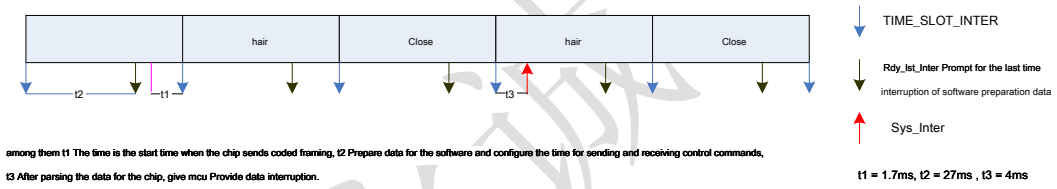


Fig 5.14 Schematic diagram of passive full-duplex transceiver

5.4.5 Application examples

The default services in Layer 2 mode include voice transmission, data transmission, voice reception, and data reception.

- Data transmission:

1 , Configuration at power on reg0x10 for 0x6A , Set the system to Layer 2 non-relay mode;

2 , After receiving the sending request (key or other methods) configuration reg0x40 for 0xA3 , Set to active mode;

3 , MCU Received one 30ms After interruption, configure reg0x41 for 0x80 , reg0x50 for 0x60 And then will soon Sent 80bit Write data frame header information HR_C6000 Sender 1.2KRAM 0x00 ~ 0x09 Address space.

4 , Next 30ms When the interruption comes, you will reg0x41 Configured as 0x00 , Idle one time slot is not sent;

5 , Next 30ms When the interruption comes, then reg0x41 Configured as 0x80 , reg0x50 Configured as 0x70 Of course Will be sent soon 96bit Write data information 1.2KRAM of 0x00 ~ 0x0b space.

6 , Repeat in turn 4 with 5 Until all required data frames and end of frame CRC32 The check digit is sent.

7 , After the data frame is sent, the next one or several 30ms After arrival, configure reg0x40 for 0x03 Turn off sending enable, End sending.

- Data reception:

1 , Configuration at power on reg0x10 for 0x6A , Set the system to Layer 2 non-relay mode; reg40 Configured as 0x43 , reg41 Configured as 0x40 , The system is busy receiving.

2 , Roger that sys_inter When reading reg0x51 with reg0x52 ,in case reg0x51 [7: 4] Equal to local cc (Defaults for 0x01) ,and reg0x51 [7: 4] equal 0x06 ,and reg0x51 [2] equal 0 , Read and receive RAM in 0x08 Low address 7bit Information, determine the total number of frames to be received next 1) , as well as RAM in 80bit The middle address information matches the local address to determine whether it is the data header that needs to be received;

3 , Next 30ms When the interruption comes, you will reg0x41 Configured as 0x00 , The next time slot is not a received job As a time slot, turn off the reception;

4 , Next 30ms When the interruption comes, you will reg0x41 Configured as 0x40 , The next time slot is the receiving time slot, Turn on reception and decrease the number of receptions at the same time.

5 , Repeat in turn 3 with 4 , The reception is decremented to 0 .

6 , In the next 30ms Interrupt, will reg0x41 Configured as 0x40 Regain busy status, if you want to close Close reg0x40 Configured as 0x03 , reg0x41 Configured as 0x20 Then configure 0x00 .

In addition, every time I receive sys_inter When reading reg0x52 with reg0x51 Determine the status and nature of each frame of data, read the receiving end RAM of 0x00 ~ 0x0B This 96bit The data gets the content of the received data frame.

- Voice transmission:

1 , Configuration at power on reg0x10 for 0x6A , Set the system to Layer 2 non-relay mode, register 0x06 Configured as 0x45 ,by MCU Control vocoder;

2 , After receiving the sending request (key or other methods) configuration reg0x40 for 0xA3 , Set to active mode;

3 , MCU Received one 30ms After interruption, configure reg0x41 for 0x80 , reg0x50 for 0x10 And then will soon Sent 80bit Voice frame header information writing HR_C6000 Sender Tx_buffer 0x00 ~ 0x09 Address space.

4 , Next 30ms When the interruption comes, you will reg0x41 Configured as 0x00 , One idle time slot is not sent, then Register 0x22 Configured as 0x80 , Turn on the vocoder coding switch.

5 , Next 30ms When the interruption comes, then reg0x41 Configured as 0x80 , reg0x50 Configured as 0x08 ,under One frame ready to send voice frame A .

6 , Next 30ms When the interruption comes, you will reg0x41 Configured as 0x00 , A free slot is not sent.

7 , Next 30ms When the interruption comes, you will reg0x41 Configured as 0x80 , reg0x50 Configured as 0x19 ,under One frame ready to send voice frame B .

8 , Repeat in turn 6 with 7 , Send the rest C, D, E, F frame reg0x50 Configured as 0x2B , 0x3B , 0x4A with 0x58 .

9 , Repeat 5 ~ 8 , Keep sending voice frames A , B , C , D , E , F Until the button is released, all superframes are sent concurrently.

10 , Received at the beginning of an idle time slot 30ms Interrupt, configure reg0x41 for 0x80 , reg0x50 for 0x20 , Ready to send the end of voice frame.

11 , Next 30ms When the interruption comes, in the next 30ms When the interruption comes, you will reg0x41 Configuration for 0x00 , Register 0x22 Configured as 0x40 , Vocoder encoding is off.

12 , After the end of the voice frame is sent, the next one or several 30ms After arrival, configure reg0x40 for 0x03 Close hair Sending is enabled, and sending ends.

- Voice reception:

1 , Configure at power on reg0x10 for 0x6A , Set the system to Layer 2 non-relay mode; reg40 Configured as 0x43 , reg41 Configured as 0x40 , The system is busy receiving.

2 ,Roger that sys_inter When reading reg0x50 with reg0x51 ,in case reg0x51 [7: 4] Equal to local cc (The default value is 0x01) ,and reg0x50 [7: 4] equal 0x01 ,and reg0x50 [2] equal 0 ,and reg0x50 [1: 0] equal 0x01 , Read and receive RAM in 0x00 ~ 0x08 information. in case addrs 0x00 The corresponding value is 0x00 , Then

With local groupaddrs versus addrs0x03 ~ addrs0x05 ;in case addrs 0x00 The corresponding value is 0x03 , Matches local srcaddrs versus addrs0x03 ~ addrs0x05 .

3 , Next 30ms When the interruption comes, you will reg0x41 Configured as 0x00 , The next time slot is not a received job As a time slot, turn off the reception, if the address matches, then configure the register 0x22 Configured as 0x20 , Turn on the vocoder decoding switch.

4 , Next 30ms When it comes, will reg0x41 Configured as 0x50 , Turn on the next time slot reception enable, same as When the voice stream output is enabled, the received voice frame is provided to the vocoder output.

5 , Next 30ms When it comes, will reg0x41 Configured as 0x00 , The next time slot is not the job of receiving Time slot, close reception;

6 , Repeat 4 with 5 Until you receive sys_inter , Read read reg0x50 with reg0x51 . in case reg0x51 [7: 4] Equal to local cc (The default value is 0x01) ,and reg0x50 [7: 4] equal 0x02 ,and reg0x50 [2] equal 0 , And reg0x50 [1: 0] equal 0x01 , Read and receive RAM in 0x00 ~ 0x08 information. in case addrs0x00 The corresponding value is 0x00 , Matches local groupaddrs versus addrs0x03 ~ addrs0x05 ;in case addrs0x00 The corresponding value is 0x03 , Matches local srcaddrs versus addrs0x03 ~ addrs0x05 . If the address matches, the configuration register 0x22 Configured as 0x10 , Turn off the vocoder decoding.

7 And next 30ms Interrupt, will reg0x41 Configured as 0x40 Regain busy status, if you want to close Close reg0x40 Configured as 0x03 , reg0x41 Configured as 0x20 Then configure 0x00 .

5.4.6 Bit error rate test

1. **Test Methods:**

HR_C6000 Continuous reception in one-layer mode 4FSK Modulated low-IF signal, the signal frequency is configurable, recommended to use 455 kHz or 450kHz IF signal. HR_C6000 Demodulate every frame 36 Byte data is stored in the receiving end 1.2KRAM Space start address is 0x30 Of the interval. MCU able to pass SPI The interface transfers each frame of data from RAM Read out and sent 36 Byte content comparison, get the error of the frame data bit Quantity. Long-term cumulative continuous test of each frame data error bit Count HR_C6000 Bit error performance.

in RAM The data stored in the data storage structure is defined as shown 5.15 As shown, MCU The frame type can be read according to the interrupt (SyncState with SyncClass (0x51)) , And read the corresponding length of data according to the frame type, and parse according to the format (The data content in the dotted frame is that it needs to be received in continuous mode CACH data).

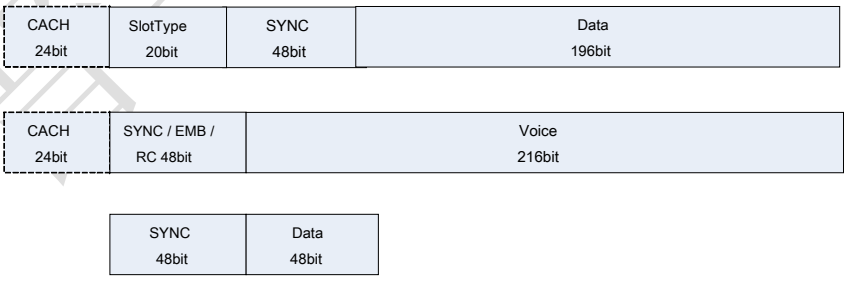


Fig 5.15 Receive data frame type format

2. **Register settings** :

To implement the bit error rate test function in one-layer mode, the registers to be configured are

table 5.6 Description of the address of the control register in the first-level mode bit error rate test

address	Configuration value	Explanation

0x01	2'bxxxx 0000 Configured for IF reception mode.	
0x07	2'b0000 1011 IF frequency word height 8 Bits, 24-bit IF frequency word divided by 2 ^ 24 Multiply 9.8304M Get the final IF frequency, the default setting is 455kHz .	
0x08	2'b1101 1001 IF frequency word 8 Bit.	
0x09	2'b0101 0100 IF frequency word low 8 Bit.	
0x10	2'b0000 0010 One-layer mode, and continuous reception, if you need time slot reception, you need to bit5 Configured as 1 .	
0x40	2'b0100 0000 Receive enable is turned on, and at the same time, it is configured into a layer test mode.	
0x41	2'b0100 0001 Receive test enable is turned on.	

6 FM application

HR_C6000 compatible FM ,stand by FM Transceiver function, through configuration register 0x10 [7] = 1'b1 So that HR_C6000 Work on FM mode. The chip is embedded with modules such as emphasis, de-emphasis, compression, and decompression. Users can choose the required functions according to their needs. In the transceiver mode, the user can choose 12.5KHz / 25KHz Channel filter, in order to prevent over-modulation, the filter has a limiter embedded.

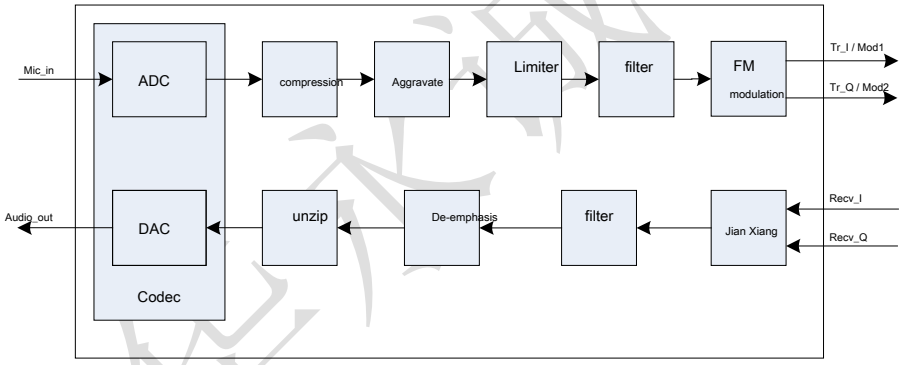


Fig 6.1 FM Block diagram of transceiver structure

6.1 FM send

In simulation mode, HR_C6000 Can only work in simplex mode, through the configuration register 0x60 = 0x80 To open the analog send channel. Voice by Codec middle ADC Sampling and converting into digital signal, after HR_C6000 After the internal optional compression and emphasis module performs audio signal processing, after 12.5KHz / 25KHz Channel filter to improve the ACPR .

The above analog channels mainly support analog voice, analog / digital subtone (CTCSS with CDCSS), DTMF , 2-tone / 5-tone with MSK Wait for voice and signaling to be sent.

- Bandpass filter

HR_C6000 Built-in optional band-pass filter, signal bandwidth is 300Hz to 3400Hz , Through the configuration register 0x34 [7] = 1'b1 , You can turn on the bandpass filter.

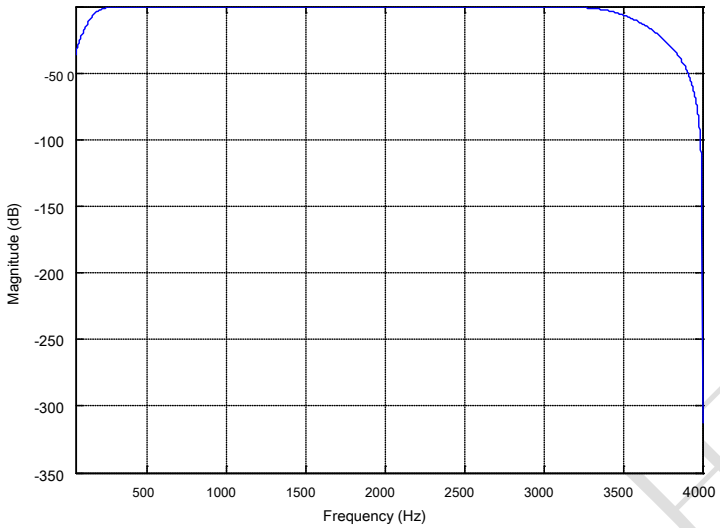


Fig 6.2 Bandpass filter spectral response

- compression

The audio compander consists of a compressor and a decompressor, which can reduce the impact of noise on audio quality. A compressor is used at the sending end to reduce the dynamic range of the audio signal by amplifying the small signal and shrinking the large signal.

HR_C6000 Adopted Syllabic Compander, according to time constant t , Change the amplitude of the signal's average envelope. The steady-state output value of the compressor is the root mean square of the input signal, that is, when the input signal increases or decreases 2dB , The output signal increases or decreases accordingly 1dB . Generally, in a voice communication system, through audio compression technology, the dynamic range can be 60dB Converted to output signal 30dB . The user can configure the register 0x34 [6] = 1'b1 , You can open the compression module. It should be noted that the compressor should be used in conjunction with decompression.

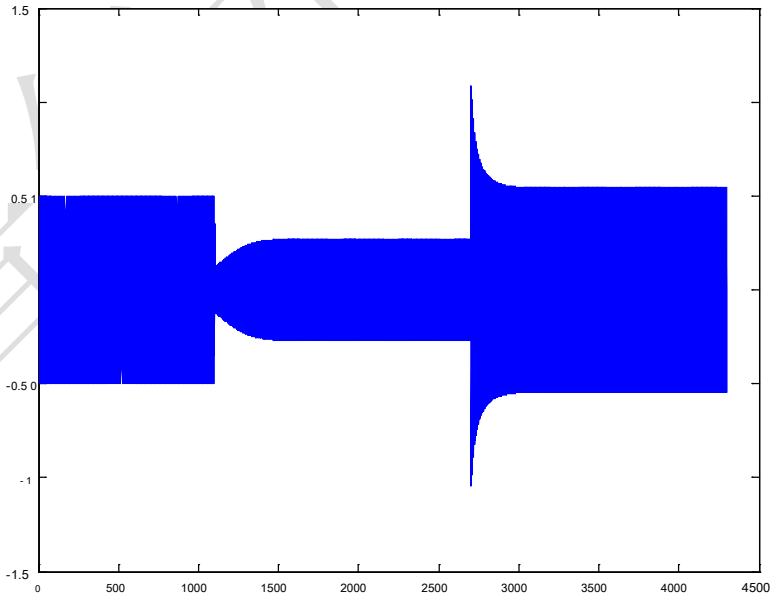


Fig 6.3 Compressed time domain response

At the same time, users can configure registers 0x2D [3: 0] To set the compressor 0dB Compression point.

- Aggravate

HR_C6000 Provide optional satisfaction TIA Required weighting module, weighting module pair 300Hz To 3000Hz Frequency band audio signal according to + 6dB / Oct Be processed. Through configuration registers 0x34 [5] = 1'b1 , You can open the emphasis module.

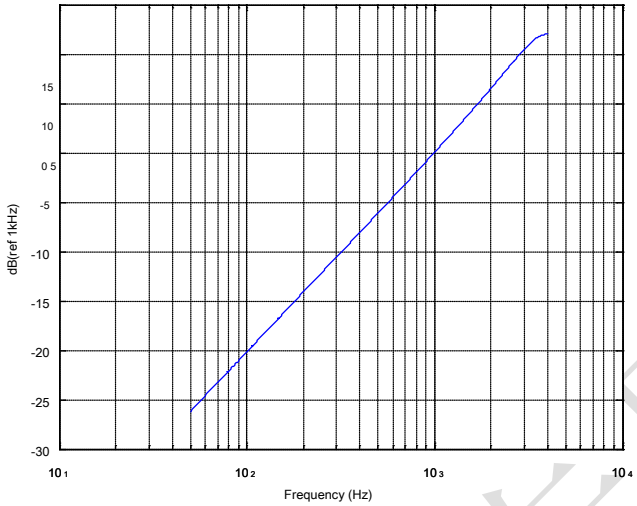


Fig 6.4 Increased frequency response curve

- filter

HR_C6000 Provide two sets of low-pass filters with built-in soft limiters, the bandwidth is 2.55KHz and 3KHz Of low-pass filters, where 2.55KHz Can be used for 12.5KHz Channel spacing to provide better ACPR index; 3KHz The low-pass filter is usually used for 25KHz Channel interval. Through configuration registers 0x34 Make a selection.

- FM Modulation HR_C6000 The transmit RF interface is configured as baseband IQ Or IF mode, you need to use HR_C6000 Internal FM The modulator performs the audio signal FM modulation. By configuration 0x3E and Mic Gain 0x0F To adjust the modulation frequency offset, and at the same time, configure the soft limit register of the transmit low-pass filter 0x3F To prevent over-modulation.

6.1.1 CTCSS send

The system is based on CTCSS Send address code (1 ~ 51) Determine the sub-audio frequency (62.5 ~ 254.1Hz), The subtone signal is generated by querying the sine table, different frequencies correspond to different addressing step lengths, and the sine data is sequentially output at the sampling clock rate through phase accumulation.

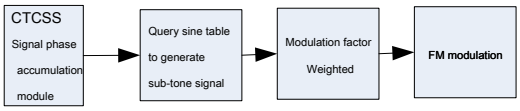


Fig 6.5 CTCSS Send block diagram

in PTT The moment the button is released, the audio signal transmission ends, and the sub-tone signal reverses phase and continues to maintain approximately 155ms To ensure that the receiving end has sufficient processing time to close the voice channel. Among them, the inversion of the subtone phase is achieved by the above-mentioned sine table addressing phase jump.

After the subtone signal is weighted by the modulation coefficient (the coefficient can be configured by the software) and the audio signal is superimposed, the FM Output after modulation.

See the attached table for detailed usage A2.2.1 .

6.1.2 CDCSS send

The transmitter first transfers the original data 12bit through golay Coded loop transmission 23bitDCS Code, and then DCS Code progress NRZ (± 1) Mapping, data input after two-stage interpolation filtering FM The modulator gets the modulation phase value and baseband modulation to form CDCSS Baseband signal output.

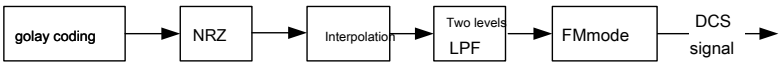


Fig 6.6 Block diagram of the sending system

See the attached table for detailed usage A2.2.2 .

6.1.3 DTMF send

DTMF Signal by 4 Group high frequency signals and 4 Group of low-frequency signals, a total of 16 Produced in a variety of ways. The low-frequency signal has a lower amplitude than the high-frequency signal 2.5dB . DTMF The signal is sent before the start of the audio signal, PTT After it becomes effective, and under normal circumstances, from PTT Press to DTMF The signal is sent, there is about 600ms The purpose of the idle state is for the receiver to have enough time to enter the detection mode. Flow Description:

versus CTCSS the same, DTMF The signal is also generated by querying the sine table. The superimposed high-frequency signal and low-frequency signal are weighted by the modulation frequency deviation coefficient, and FM Output after modulation. Each DTMF Code correspondence 50ms Signal length, followed by 50ms of IDLE status. DTMF The supported encoding length is determined by the user.

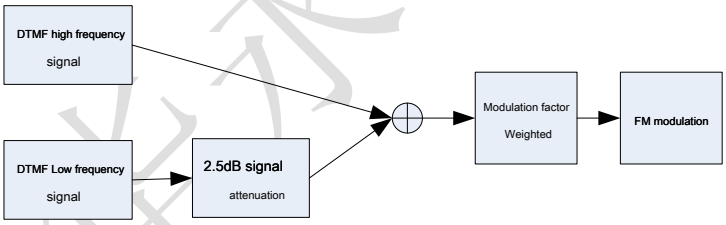


Fig 6.7 DTMF Send block diagram

See the attached table for detailed usage A2.2.3 .

6.1.4 2-tone send

2-tone The signal has in-band tone signal and IDLE The gap constitutes a sequence of tones, with EIA Take the standard as an example, the duration of each group of tones is 33ms , IDLE The gap is 0 . However, considering the compatibility with other standards, the signal length and IDLE The software for the gap length can be configured. As shown in the figure below, with the cooperation of the timing module and the channel IDLE Gap switching.

Selcall tone happened at PTT After pressing, before the audio signal is transmitted. Selcall tone Weighted by modulation factor and FM Output after modulation.

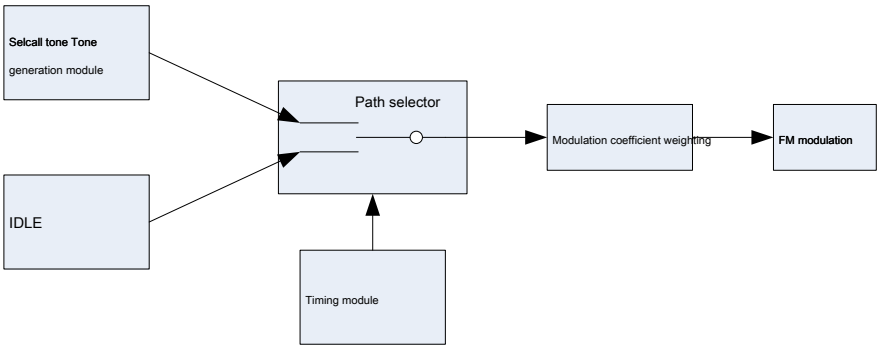


Fig 6.8 2-tone Send block diagram

See the attached table for detailed usage A2.2.4 .

6.1.5 5-tone send

5-tone 'S sending process with 2-tone The same, distinguished by different register control bits. See the attached table for detailed usage A2.2.5 .

6.2 FM receive

When the configuration register 0x60 = 0x00 , HR_C6000 Is in receive mode. HR_C6000 To the received IQ (Or intermediate frequency) signal is filtered and phase-detected and sent to FM Processing module. The signal after phase detection is filtered by the audio filter, and then processed by the optional de-emphasis and decompression module, Codec Output.

The above analog channels mainly support analog voice, analog / digital subtone (CTCSS with CDCSS), DTMF , 2-tone / 5-tone with MSK Wait for voice and signaling reception.

- filter

HR_C6000 in FM Two sets of low-pass filters are provided in the receiving and processing channel with a bandwidth of 2.55KHz and 3KHz Of low-pass filters, where 2.55KHz Can be used for 12.5KHz Channel spacing 3KHz The low-pass filter is usually used for 25KHz Channel interval. Can be configured 0x34 Register selection.

- De-emphasis

HR_C6000 Provide optional satisfaction TIA De-emphasis module required, de-emphasis module pair 300Hz To 3000Hz The audio signal of the frequency band according to- 6dB / Oct Be processed. Through configuration registers 0x34 [5] = 1'b1 , You can open the de-emphasis module.

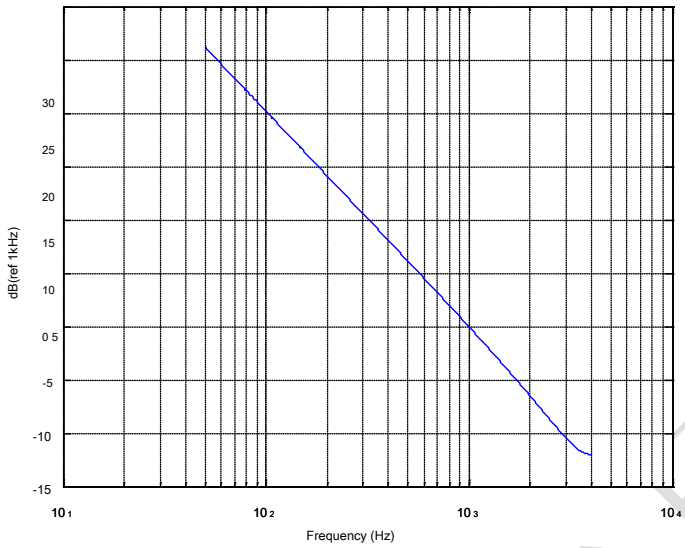


Fig 6.9 De-emphasis frequency response curve

- unzip

A decompressor is used at the receiving end to increase the dynamic range of the audio signal by reducing the large signal and amplifying the small signal.

The steady-state output value of the decompressor is the square of the input signal, that is, when the input signal increases or decreases 1dB , The output signal increases or decreases accordingly 2dB . Generally, in a voice communication system, through audio compression technology, the dynamic range can be 30dB Converted to output signal 60dB . The user can configure the register 0x34 [6] = 1'b1 , You can open the compression module.

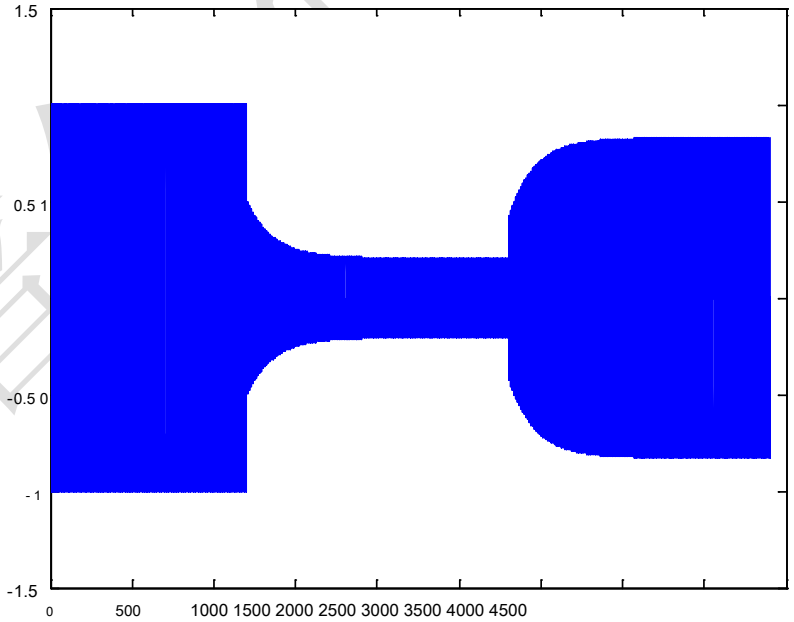


Fig 6.10 Decompress time domain response

At the same time, users can configure registers 0x2D [7: 4] To set the compressor 0dB Compression point.

- Bandpass filter

HR_C6000 in FM The receiver has a built-in optional band-pass filter, and the signal bandwidth is 300Hz to 3400Hz , Through the configuration register 0x34 [7] = 1'b1 , You can turn on the bandpass filter.

6.2.1 CTCSS receive

CTCSS The air signal generates phase information through the phase detector, and the frequency offset calibration module eliminates the DC offset of the signal. 4 Order IIR 300Hz The low-pass filter filters out high-frequency audio.

The frequency response amplitude detection result is compared with the preset threshold value. If the threshold value is exceeded, the voice enable is turned on, and an interrupt signal is output to notify the peripheral device to open the speaker and the voice path.

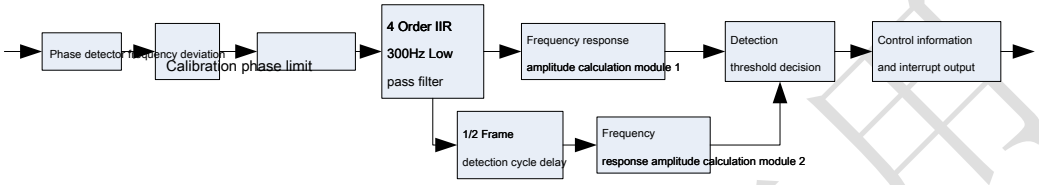


Fig 6.11 CTCSS Receive block diagram

See the attached table for detailed usage A2.2.1 .

6.2.2 CDCSS receive

CDCSS Modulation includes FM The demodulation module adopts a non-coherent demodulation scheme. CDCSS Signal reception includes differential phase discrimination, frequency offset estimation, and decision, golay Decoding and other key steps. The flow of back-end baseband processing is shown in the figure 6.12 As shov

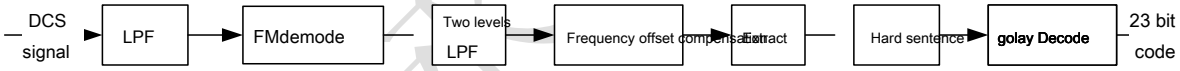


Fig 6.12 Receiving baseband processing flow chart

CDCSS The baseband signal is filtered through a low-pass filter to remove part of the out-of-band noise. FM Demodulation is restored to the amplitude value, and then the next two levels LPF After further filtering out noise and audio signals, frequency offset compensation is performed; 7 Hard decision on double symbol rate golay Decode to select the best way.

See the attached table for detailed usage A2.2.2 .

6.2.3 DTMF receive

DTMF The demodulation process is to analyze the frequency distribution of the air signal, according to DTMF Combined reverse decoding. Calculate the air signal at 8 The frequency response amplitude of the group frequency is selected, and the maximum amplitude in the high frequency part and the maximum amplitude in the low frequency part are selected respectively. The combination of the two can be determined DTMF code.

Each group DTMF After decoding, a system interrupt will be generated, and an indication DTMF Check whether the end flag information. After receiving the interrupt, the peripheral DTMF The code is stored in a cache area. When an interruption comes and the detection end flag information is valid, all the previously saved DTMF The code forms a frame output.

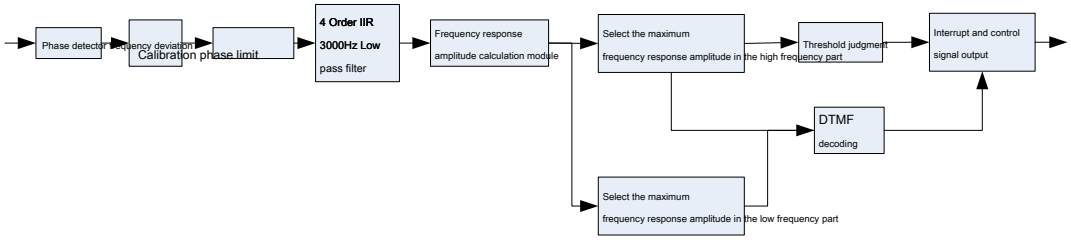


Fig 6.13 DTMF Receive block diagram

See the attached table for detailed usage A2.2.3 .

6.2.4 2-tone receive

2-tone The demodulation mechanism is similar to address matching, only when 2-tone The voice channel can be opened only when it matches the receiving address setting. 2-tone Contains two sets of tones or a set of long tones, so whenever the match is correct once, the demodulation coefficient is set to the corresponding value of the next set of reception frequencies. In addition, a timeout mechanism has been added to the module. If the frequency cannot be matched for a long time, the previous result is cleared and the matching process restarts.

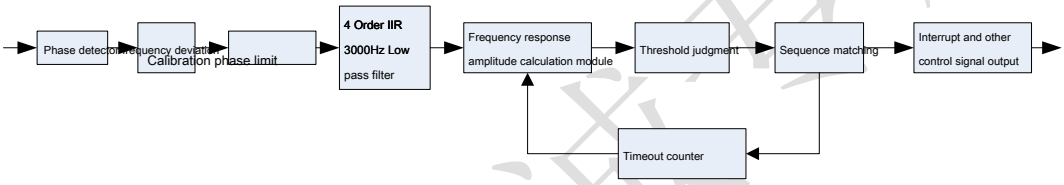


Fig 6.14 2-tone Receive block diagram

See the attached table for detailed usage A2.2.4 .

6.2.5 5-tone receive

5-tone Of the receiving process with 2-tone The same, distinguished by different register control bits. See the attached table for detailed usage A2.2.5 .

7 MSK Application note

7.1 MSK send

MSK Sending will first frame the information data according to the frame structure requirements, and then send the data into the map interpolation MSK Modulate, and then pass the modulated data through NCO Move to 1.5KHz On the mid-range, MSK And spectrum transfer in one module Into a continuous phase signal, which is finally input to FM modulation. In this way, the entire data modulation process is completed.

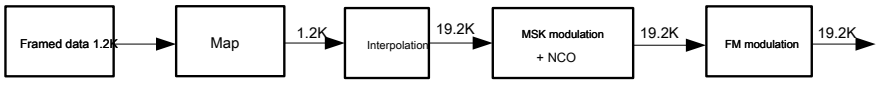


Fig 7.1 Block diagram of the sending system

7.2 MSK receive

MPT1327 Proposed MSK Modulation contains a FM Modulator, so the design of the receiver is inverse to the modulation process, plus

Enter FM The demodulation module adopts a non-coherent demodulation scheme. The receiver is divided into front-end data acquisition and back-end baseband signal processing.

The front-end data collection part is similar to the processing of the second half of the sender, and will not be described here. The back-end signal processing part arrives

The key steps such as detection, timing synchronization, and judgment are all completed in this part. MSK The flow of baseband processing is shown in the figure 7.2 As shown.

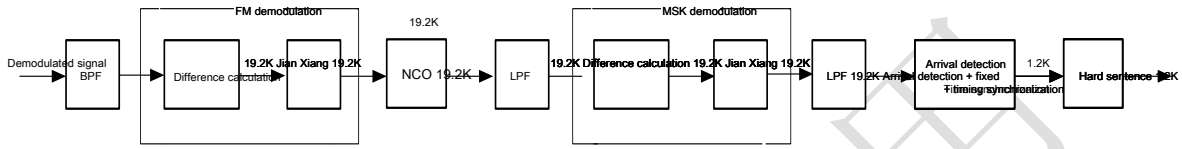


Fig 7.2 Receiving baseband processing flow chart

The receiver design uses non-coherent demodulation and uses the front-end data acquisition module to obtain two basebands IQ Signal, then proceed

Differential phase detection, and then sent to a low-pass filter to eliminate out-of-band noise, and finally the back-end signal processing.

7.3 MCU Instructions for use

7.3.1 MCU work process

7.3.1.1 initialization

MCU Initialization, configuration register TrainErrorThreshold for 5 , DTBeforeTransAndRec for 160 ,
Channel_Delay for 20 , NT for 103

7.3.1.2 Send control

- Control channel transmission

  MCU When it is necessary to send data, when the interruption of the reception time slot is detected, the transmission ping-pong buffer is filled first,

and then the register is configured OperationType for 1 , ChannelType for 0 , TranOrRecFlag for 1 , MacFrameEn (MAC When framing 1 , PHY When framing 0), Unsolicited for 0 , MultiMessageTransFlag for 0 . MAC When a half-full interrupt of ping-pong buffer is received, there are two cases:

  - PHY Framing. The data sent each time is 64 Bit. If there are still bits of data that have not been sent, continue to send 64 Bit. If there is no data to send, then yes MACTransFinishFlag Set 1 .
  - MAC Framing. The previous data is every time 64 Bits, the last data sent may be less than 64 Bit. If there are still bit data not sent, then continue to send. If it is the last time to send data then yes

    MACTransFinishFlag Set 1 , Send data and configure at the same time RemBitNum Is the length of the remaining data bits.

- Traffic channel transmission control

  MCU When you need to send data, fill the sending ping-pong buffer first, then MCU Configuration register OperationType for

1 , ChannelType for 1 , TranOrRecFlag for 1 , MacFrameEn (MAC When framing 1 , PHY When framing

0), Unsolicited for 1 . MAC When a half-full interrupt of ping-pong buffer is received, there are two cases

- PHY Framing. The data sent each time is 64 Bit. If there are still bits of data that have not been sent, continue to send 64 Bit. If there is no data to send, then yes MACTransFinishFlag Set 1 . If the multi-frame message is sent and the first message is sent, then the correct MultiMessageTransFlag Set the register to one and send the next message 64 Bit data.

- MAC Framing. The previous data is every time 64 Bits, the last data sent may be less than 64 Bit. If there are still bit data not sent, then continue to send. If it is the last time to send data then yes MACTransFinishFlag Set 1 , Send data and configure at the same time RemBitNum Is the length of the remaining data bits.

- Data channel transmission control

  Data channel transmission control is the same as control channel transmission, except that ChannelType Set to 2

7.3.1.3 Receive control

- Control channel reception

  MCU When you need to receive a receipt, configure the register OperationType for 1 , ChannelType for 0 , TranOrRecFlag for 0 , AcqEnable for 1 , RxInterMask for 0 , CtrlDataInterMask for 0 . MCU The receiving interrupt handler reads the register value after detecting the receiving terminal pulse RecBitLen , TrainCodewordFlag with TrainErrorBitNum), And read the data of corresponding length according to the register value.

- Traffic channel reception

  MCU When you need to receive a receipt, configure the register OperationType for 1 , ChannelType for 1 , TranOrRecFlag for 0 , AcqEnable for 1 , RxInterMask for 0 , CtrlDataInterMask for 0 . MCU Receive interrupt handler After detecting the receiving terminal pulse, read the register value (RecBitLen , TrainCodewordFlag with TrainErrorBitNum), And read the data of corresponding length according to the register value.

- Data channel reception

  MCU When you need to receive a receipt, configure the register OperationType for 1 , ChannelType for 2 , TranOrRecFlag for 0 , AcqEnable for 1 , RxInterMask for 0 , CtrlDataInterMask for 1 . MCU Receive interrupt handler After detecting the receiving terminal pulse, read the register value (RecBitLen , TrainCodewordFlag with TrainErrorBitNum), And read the data of corresponding length according to the register value.

7.3.2 Reset operation

When you need to recapture, you can use the configuration register SoftRest First for 1 Again for 0 Reset the physical layer.

7.4 Parameter configuration

7.4.1 Basic parameter configuration

1) Capture and synchronization decision threshold

2) Delay between receiving pulse and transmitting start pulse.

3) NT

table 7.1 Basic parameter configuration

address	name	Default value definition		Explanation
0x12A	TrainErrorThreshold		Bit7-Bit6 Keep Bit5-Bit0 During capture and synchronization	Training sequence decision threshold.
0x12B	DTBeforeTransAndRec			The delay between receiving the pulse and transmitting the start pulse. The value configured here is 19.2kHz The sampling clock is the base value. Assuming that the configuration value is n , The delay time is n / 19.2 millisecond.
0x12C	NT			MAC Delay difference from framing to the start of air interface transmission
0x12D	ChannelDelay			Traffic channel TSC The maximum delay (in bits) in response to an active message from the mobile station.

7.4.2 MAC Parameter configuration issued

1) Whether to capture the message (AcqEnable).

2) What channel is the current channel message (control channel, traffic or data channel, Channel Type).

3) The current time slot is the message sent or received (TranOrRecFlag).

4) Working mode (working or idle state, OperationType).

5) The message with the remaining data length of the transmitted bit. Framing is divided into MAC Framing and PHY Framing, in MAC Framing

In this case, since the total number of bits is not necessarily 64 Multiple (including link establishment time, etc.), so when the number of transmitted bits is small

to 64 Bit time must be informed PHY How many bits are left unsent (RemBitNum).

6) Software reset message (SoftRest).

7) Multi-information frame transmission message (MultiMessageTransFlag), When transmitting multiple information frames, at the intersection of the two information

Before the flip bit is inserted at the boundary, this message is given, PHY Given when framing, MAC The framing need not be given.

8) Receive interrupt mask message (RxInterMask).

9) Control data interrupt mask message (CtrlDataInterMask).

10) The framing method is determined by MAC Framed by PHY Framing (MacFrameEn).

11) MAC End of transmission message (MACTransFinishFlag).

12) Actively send frame information (Unsolicited). It is valid when the traffic channel is sent.

table 7.2 MAC Deliver parameter configuration

address	name	Default value	definition	Explanation
0xd5	AcqEnable		Bit7	1 : PHY Perform the capture operation. 0 : Does not work. Note: This information works for the up jump, so PHY Read AcqEnable Be MAC Set 1 After that, immediately clear 0 .
	OperationType		Bit6	0 : Indicates idle state. 1 : Indicates the working state.
	ChannelType		Bit5- Bit4 The base station is used as the transmission channel type.	use 00 : Control channel. 01 : Business channel. 10 : Data channel. 11 : Reserved.
	TranOrRecFlag		Bit3	0 :receive. 1 :send.
	SoftReset		Bit2	The base station serves as a reset signal for the sending module The station performs both reset and reset 0 : Does not work. 1 : Reset.
			Bit1- Bit0 Keep	
0xd6			Bit7- Bit6 Keep	

	RemBitNum		Bit5- Bit0 MAC Unsent Bit Bit. range 0-63 .	
0xd7 MultiMessageTransFlag			Bit7	0 : Does not work 1 : After the current codeword is sent, the flip bit should be added. Note: This information works for the up jump, so PHY Read AcqEnable Be MAC Set 1 After that, immediately clear 0 . And only PHY Framing is valid.
	RxInterMask		Bit6	0: Does not work. 1: Receive interrupt mask.
	CtrlDataInterMa sk		Bit5	0: Does not work. 1: Receive interrupt mask.
	MacFrameEn		Bit4	0 : PHY Framing. 1 : MAC Framing.
	MACTransFinishFlag		Bit3	0 : Does not work. 1 :Correct PHY In framing, after the current codeword is fetched, the bit data fetching ends. Correct MAC For framing, the current codeword is taken and then taken RemBitNum After the length, the bit data acquisition ends.
	Unsolicited		Bit2	0 : Send response information. 1 : Send information actively.
	msk_voice_send _en		Bit1	0 :send MSK Signaling information. 1 :send FM voice.
			Bit0	Keep
0xd8	ChannelType_R X		Bit1- Bit0 The base station as the receiving channel type, the mobile station does not use 00 : Control channel. 01 : Business channel. 10 : Data channel. 11 : Reserved.	
	SoftReset_RX		Bit2	The base station serves as a reset signal for the receiving module Taiwan does not use 0 : Does not work. 1 : Reset.
			Bit7- Bit3 Keep	

7.4.3 MAC Obtained parameter configuration

1) Interrupt message (CtlDataInterpType). PHY give MAC The interruption can be multiple, a total of two

Interrupt pins, one of which is the receive time slot interrupt (receive demodulation interrupt is replaced by the receive time slot interrupt, by adding registers

The flag bit judges whether the current data is valid or not. The other one is the control data interrupt (the interrupt includes sending the ping-pong buffer half full

Interrupt and PHY Transmit end interrupt, distinguish by register vector).

2) Received data length (RecBitLen). Received data length is divided into 128 Bit sum 64 Bit. Number of receptions during capture

According to the length 128 Bit. The received data length during synchronization is 64 Bit.

3) Synchronous sequence code word mark (TrainCodewordFlag). This news is telling MAC The currently resolved codeword is

Does it have a synchronization sequence. When the received data length is 128 Bits, this message can be ignored.

4) Number of bit errors in the synchronization sequence (TrainErrorBitNum). When the received data length is 128 Bit or sync sequence code

The word mark is 1 This data is valid at the time.

table 7.3 MAC Get parameter information

address	name	Default value	definition	Explanation
0x96	RecBitLen		Bit7- Bit0 The length of the received data bits.	
0x97			Bit7- Bit6 Keep	
	TrainCodewordFlag		Bit5	0 : Data codeword. 1 : Code word with synchronization sequence.
	TrainErrorBitNum		Bit4- Bit0 Indicates the number of error bits in the training sequence (range 0 — 31). only in TrainCodewordFlag for 1 Is only valid when it is available.	

8 Register description

table 8 .1 System parameters Number

table type address Read and write		name	Default value definition		Explanation
Reset	0x00 W DMRnRst			Bit7	for 0 Reset DMR Protocol, valid within a system clock, HR_C6000 It is automatically cancelled internally and the following reset processing is the same.
		PHYnRst	0x00	Bit6	for 0 Reset the physical layer
		CodernRst		Bit5	for 0 Reset codec
		FMnRst		Bit4	for 0 Reset FM
		VoCoderRst		Bit3	for 0 Reset vocoder interface
		MSKRst		Bit2	for 0 Reset MSK Module
		IISRst		Bit1	for 0 Reset I2S interface
		CodeCRst		Bit0	for 0 Reset when built-in CodeC , 3 Valid within one system clock, HR_C6000 Internal automatic revocation
Hardware Configuration	0x01 W / R RFTransIQMode		0xb0	Bit7	IQ In mode: 0 : Indicates the sender I Road in DAC of I Road output Q Road in DAC of Q Road output 1 : Indicates the sender I Road in DAC of Q Road output Q Road in DAC of I 路 Output. In two-point mode: adjust the modulation frequency offset mapping relationship, see 4.7.2 Instructions.
		RFRecvIQMode		Bit6	0 : Indicates the receiving end I Road in ADC of I Input, receiver Q Road in ADC of Q Road input 1 : Indicates the receiving end I Road in ADC of Q Input, receiver Q Road in ADC of I 路 input.
		RFTransMode		Bit5-Bit4	00 Means to send IF mode, 01 Means sending intermediate frequency IQ mode, 10 Indicates the transmit baseband IQ mode, 11 To send two-point modulation mode
		RFRecvMode		Bit3-Bit2	00 Indicates receiving IF mode, 01 Indicates receiving intermediate frequency IQ mode, 10 Receiving baseband IQ mode
				Bit1	IQ Road balance debugging, 1 Indicates that the signal is sent 0 Add the offset value, 0 Expressed as normal
				Bit0	control ADC with DAC The phase of the module input clock is enabled and configured as 1 At this time, the clock is opposite to the system clock, otherwise it is the same.

	0x02 W / R TransIsigCenter		0x00	Bit7-Bit0	IQ In mode: send I Road offset value, if RFTransIQMode for 0 , Then the offset is added to DAC of I Road, otherwise it should be added DAC of Q Road; in two-point mode: adjust the output MOD2 Road offset, the adjustment range is about ± 422mV , The minimum adjustment step is 3.3mV .
	0x03 W / R RecvIsigCenter		0x00	Bit7-Bit0	receive I Road offset value, if RFRecvIQMode for 0 , Then the offset is added to ADC of I Road, otherwise it should be added ADC of Q road;
	0x04 W / R TransQsigCenter		0x00	Bit7-Bit0	IQ In mode: send Q Road offset value, if RFTransIQMode for 0 , Then the offset is added to DAC of Q Road, otherwise it should be added DAC of I Road; in two-point mode: adjust the output MOD2 Road offset, the adjustment range is about ± 422mV , The minimum adjustment step is 3.3mV .
	0x05 W / R RecvIsigCenter		0x00	Bit7-Bit0	receive Q Road offset value, if RFRecvIQMode for 0 , Then the offset is added to ADC of Q Road, otherwise it should be added ADC of I road
	0x06 W / R Vocoder		0x40	Bit7-Bit6	00 select V_SPI Vocoder 01 select AMBE3000 11 select AMBE1000
		DMRFrom		Bit5	0 Means to choose two vocoders (AMBE3000, AMBE1000) One of them is output as a source code, 1 Pass V_SPI The vocoder code output connected to the universal interface.
		VocoderFrom		Bit4	0 Represents the voice codec package to DMR Protocol layer processing, at this time, the vocoder works normally in the voice sending state; 1 Denotes that the voice encoding is sent directly to the vocoder for decoding buffer ; At this time, the vocoder is working in the self-loop test state.
		SPIFrom		Bit3	0 Means generic V_SPI Interface from DMR The protocol layer of the chip reads the voice data, at this time the vocoder works normally in the voice receiving state; 1 Means generic V_SPI Interface directly from DMR The chip's vocoder reads the codec package. At this time, the vocoder works in voice recording.
		CodeCMode		Bit2	0 Means built-in, 1 Means external

			OpenMusic		Bit1	1 Open for playing boot sound or incoming call reminder, etc., 0 shut down
			LocalVoCoderControl		Bit0	0 Indicates that the system is automatically controlled, 1 Express MC Control the switch of the vocoder
	0x07 W / R IFFreq2			0x0B Bit7-Bit0 IF frequency word height 8 Bit, twenty four Bit Intermediate Frequency Rate word divided by 2 ^ 24 Multiply 9.8304M Get the final IF frequency.		
	0x08 W / R IFFreq1			0xB8 Bit7-Bit0 IF frequency word 8 Bit		
	0x09 W / R IFFreq0			0x00 Bit7-Bit0 IF frequency word low 8 Bit		
	0x0A W / R Clk_enb			0x81 Bit7		Clock switch control bit. The internal clock is switched from the crystal clock to PLL The output clock control bit of the high level indicates that the internal clock directly clocks the crystal oscillator and changes the configuration reg0x0B w reg0x0C Then you need to wait for greater than 500μs In order to switch the internal clock from the crystal back PLL Output.
					Bit6-Bit1 Keep	
					Bit0	HR_C6000 of CLKOUT Pin clock output control is enabled.
	0x0B W / R PLLM			0x28 Bit7-Bit0		PLL M register
	0x0C W / R PLLBP				Bit7	0 Indicates use PLL , 1 Express PLL bypass
			PLL SLEEP	0xB3	Bit6	Keep
			PLLDO		Bit5-Bit4	PLL Output frequency
			PLLN		Bit3-Bit0	PLL Enter the frequency divider
	0x0D W / R Voice_superframe			0x02 Bit7-Bit4 Keep		Bit3-Bit0 Voice anomaly detection Superframe length waiting to exit Degrees, the actual internal detection time is (Voice_superf + 1) * 360ms
	0x0E W / R Keep					
	0x0F	R	FSKErro		Bit7-Bit0 statistics FSKErro or EVM Value	Get effective when the time slot is interrupted.
System parameter configuration	0x10 W / R ModulatorMode			0x73 Bit7		0 Express DMR , 1 Express FM
			TierMode		Bit6	0 Express TierI , 1 Express TierII
			ContinueMode		Bit5	0 Express Continue , 1 Express TimeSlot . In Layer 2 mode, need to receive CACH Information bit Set 0 .
			LayerMode		Bit4-Bit3	00 Indicates the physical layer mode, 01 Indicates the second layer mode, 10 Represents the third layer mode
			ISRepeater		Bit2	0 Means non-relay, 1 Means relay
			ISAligned		Bit1	0 Means offset (offset mode in non-relay mode means single frequency relay) 1 Indicates alignment
			RepeaterSlot		Bit0	In three-layer mode: must be configured as 1 ;

					In Layer 2 mode: 0 Express Slot1 , 1 Express Slot2
	0x11 W / R LocalChanMode		0x80	Bit7	Set 1 effective. In relay mode RepeatedSimplex ; Expressed in direct mode DirectSimplex
				Bit6	Set 1 effective. In relay mode RepeatedDuplex ; Expressed in direct mode DirectDuplex
				Bit5	
				Bit4	
				Bit3	
				Bit2	
				Bit1	
				Bit0	Set 1 It means that the digital and analog simultaneously receive the opening control enable, set 0 Indicates that only digital or analog reception is enabled.
	0x12 W / R rf_pre_on		0x00 Bit7		Enables smooth rise and fall of signal strength at the time slot boundary
				Bit6	Two-point modulation test is enabled, the bit Enable, DAC Terminal output 40Hz Sine wave.
				Bit5-Bit0 The amount of radio frequency switching from receiving to sending interruption ad	Step size is about 100μs . The amount of interrupt advance from switching to receiving is in the register 0xC0 Definition.
	0x13	W Cend_band	0x00 Bit7-Bit4		rf_tx_en or rf_rx_en Valid to invalid 30ms Advancement of the boundary, 100μs The interval is increased by the step size, and the maximum value is configured not to exceed 11 * 100μs , Valid only in discontinuous mode.
				Bit3-Bit0 Rf_tx_en or rf_rx_en Invalid to valid	Hou Relative 30ms The amount of delay at the boundary, to 100μs The interval is increased by the step size, and the maximum value is configured not to exceed 11 * 100μs , Valid only in discontinuous mode.
	0x14 W / R LocalSreAdrressL		0x01 Bit7-Bit0 Local address is low 8Bit		
	0x15 W / R LocalSreAdrressM		0x00 Bit7-Bit0 Local address 8Bit		
	0x16 W / R LocalSreAdrressH		0x00 Bit7-Bit0 Local address is high 8Bit		
	0x17 W / R LocalGroupAdrressL		0x33 Bit7-Bit0 The local group address is low 8Bit		
	0x18 W / R LocalGroupAdrressM		0xef	Bit7-Bit0 In the group address of this machine 8Bit	
	0x19 W / R LocalGroupAdrressH		0x00 Bit7-Bit0 The local group address is high 8Bit		
	0x1A W / R LocalBSAdrressL		0xff	Bit7-Bit0 Local BS Low address 8Bit	
	0x1B W / R LocalBSAdrressM		0xff	Bit7-Bit0 Local BS In address 8Bit	
	0x1C W / R LocalBSAdrressH		0xff	Bit7-Bit0 Local BS High address 8Bit	

	0x1D W / R	LocalUnaddress	0xff	Bit7-Bit4	No address to receive address
		MaskUnaddr		Bit3-Bit0	No address call matching code, the matching code is 1 Correspondence bit It is ignored when the address matches, that is, the bit is not compared.
	0x1E W / R	LocalBroadCast	0xff	Bit7-Bit4	Broadcast receiving address
		MaskBroadCast		Bit3-Bit0	All call (broadcast) matching code, the matching code is 1 Correspondence bit When the address matches To ignore, that is, no comparison is made to this bit.
	0x1F W / R	LocalEMB	0x10	Bit7-Bit4	local CC Set up
				Bit3	PI Bit setting
				Bit2	
				Bit1-Bit0	EMB region PI Encrypted information and post-access letter The ratio of the number of times of interest changes. 00 Indicates that there is no encrypted information; 01 Express 1 : 1 ; 10 Express 2 ; 11 Express 1 : 4
	0x20 W / R	LocalAccessPolicy	0xAA	Bit7-Bit6	00 Express impolite , 01 Express polite to all , 10 Express polite to cc .
				Bit5-Bit4	versus Bit7-Bit6 the same
				Bit3-Bit2	versus Bit7-Bit6 the same
				Bit1-Bit0	versus Bit7-Bit6 the same
	0x21 W / R	LocalAccessPolicy1	0xA0	Bit7-Bit6	versus Bit7-Bit6 the same
				Bit5-Bit4	versus Bit7-Bit6 the same
				Bit3	Confirm package feedback polite Strategy, 0 Express impolite , 1 Express polite
				Bit2	Keep
				Bit1	Clear vocoder encoding cache buffer The control of the data in the bit for 1 After clearing this buffer Value in, then the system will automatically reply bit for 0
				Bit0	Clear vocoder decoding cache buffer The control of the data in the bit for 1 After clearing this buffer Value in, then the system will automatically reply bit for 0
	0x22 W / R	EncodeStart	0x01	Bit7	Write 1 Indicates the start of vocoder coding
		EncodeStop		Bit6	Write 1 Indicates the end of vocoder coding
		DecodeStart		Bit5	Write 1 Indicates the start of vocoder decoding
		DecodeStop		Bit4	Write 1 Indicates the end of vocoder decoding
				Bit3	Keep
		sel_I2S_mode		Bit2	select I2S Master-slave mode bit for 1 , Indicates interface with vocoder I2S Master mode, otherwise slave mode. The bit Only if sel_I2StoI2S The control bit is set to 1 Only effective afterwards.

			sel_I2StoI2S		Bit1	Select transmission with vocoder PCM The data interface is I2S The interface is still SPI interface. The bit for 1 Then choose yes I2S Interface, otherwise bit SPI interface.
			Ambe1000_noise_enb		Bit0	AMBE1000 Squelch is enabled, 0 The squelch function is invalid.
	0x23 W / R				Bit7-Bit0 Keep	
	0x24 W / R			0xF8 Bit7-Bit2 Keep		
			AMBE1000FrameRept		Bit1	AMBE1000 Frame repeat
			AMBE1000ForceSilen		Bit0	AMBE1000 Force decoder to mute
Vocoder SPI Scale parameter	0x2A W / R	spi_clk_cnt		0x0B Bit7- Bit0 C_SPI Clock = Codec clock / [2 * (spi_clk_cnt + 1)]		
FM	0x2B R		Sql_l	0x00 Bit7- Bit0 FM In mode, the squelch signal is low 8bit		
	0x2C R		Sql_h	0x00 Bit7- Bit0 FM In mode, the squelch signal is high 8bit		
	0x2D W / R	shift_radix		0x0B Bit7- Bit4 For configuration FM Uncompressed in mode 0dB Gain point		
					Bit3- Bit0 For configuration FM Compressed in mode 0dB Gain point	
	0x2E W / R	tx_pre_on		0x04 Bit7- Bit5 Keep	Bit4- Bit0 Send advance configuration value, due to RF channel Delay is different, in order to ensure the air DMR The signal is strictly 30ms The time slot boundary is sent. By configuring this register, the delay amount of the RF channel is offset, and the delay unit value is 100us . If the configuration value is 0x04 , It means to send advance configuration 400us .	
Codec Interface parameters	0x2F W / R	par_ck_cnt		0x00 Bit7- Bit0 Configure Vocoder I2S Interface in main mode Clock frequency (I2S_CK_M). The calculation method is: I2S_CK_M = codec working frequency/(2 * (par_ck_cnt +1)) , And I2S_CK_M Requirements greater than 272KHz .		
	0x32 W / R	LRCK_CNT_H		0x02 Bit7- Bit0 Codec In active mode, configure I2S_FS_M The clock frequency is calculated as: I2S_FS_M = codec working frequency / [2 * (LRCK_CNT + 1)] And must guarantee I2S_FS_M = 8KHz .		
	0x33 W / R	LRCK_CNT_L		0xff	Bit7- Bit0	
FM	0x34 W / R	FMBpfOn		0xbe	Bit7	0 Indicates that the bandpass filter is off, 1 Means open
			FMCompressorOn		Bit6	0 Means compression is off, 1 Means open
			FMPreEmphasisOn		Bit5	0 Indicates that pre-emphasis is off, 1 Indicates that pre-emphasis is on
			FMBandWidth		Bit4	FM Send bandwidth selection, 0 Express 12.5K ,

						1 Express 25K
			FMBandWidth_adj		Bit3	FM In mode, baseband IQ And IF, IF IQ During transmission, the bandwidth selection of the transmission adjacent channel suppression filter. 0 Express 12.5KHz bandwidth, 1 Express 25KHz bandwidth
			FMBandWidth_r		Bit2	FM Receive bandwidth selection, 0 Express 12.5K , 1 Express 25K
			FMBandWidth_ctc		Bit1	Yayin CTCSS Receive bandwidth selection, 0 Express 12.5K , 1 Express 25K
					Bit0	Keep
	0x35 W / R FM_dev_coef_t			0x14 Bit7- Bit0 FM Origin modulation frequency deviation coefficient		
	0x36 W / R mcu_alc_clk_down			0x00 Bit7		External Codec of BCLK with LRCK Close enable, high effective
			mcu_vspi_clk_down		Bit6- Bit5 Vocoder C_SPI Interface SCK Clock off Close enable. 2'bx1 Time, SCK Always off 2'b00 Time, SCK The clock is always on; 2'b10 Time, according to SPI Interface CS State determination SCK Whether to close CS In the active state (low level), then SCK The clock is on, otherwise SCK The clock is off. When to use I2S Interface as vocoder PCM When transmitting the interface, bit6 Also defined as control I2S_CK with I2S_FS Enable switch. Bit6 for 1 Time, turn on the use of these two clocks Yes, otherwise turn off the two clock enable.	
			mcu_vspi_cs_down			
			mcu_pkt_clk_down		Bit4	Vocoder codec data packet interface clock is off and enabled, high effective
			mcu_ctr_rst1000		Bit3	Whether by mcu control AMBE1000 of reset , 0 Indicates that the system is automatically controlled, 1 Express mcu control
			mcu_val_rst1000		Bit2	mcu Set up AMBE1000 of reset signal, 1 Indicates high level
					Bit1	FM Receiving and opening the voice channel in mode Codec switch, 1 Means open 0 Means off.
					Bit0	Keep
	0x37 W / R mcu_control_shift			0x00 Bit7		mcu Control built-in and external Codec of DACDATA Variety, 0 Means unchanged, 1 Express change
			zoom		Bit6	in mcu_control_shift for 1 In the state of 0 Means smaller, 1 Means bigger
					Bit5	0

			shift_size		Bit4- Bit0 Built-in or external Codec of DACDATA variation range, 5'b00001-5'b11111 Express DACDATA Gradually increase, the change step is 1.5dB .	
FM	0x3e W / R FM_dev_coef_r			0x08 Bit7- Bit0 FM Modulation frequency deviation coefficient at the receiving end		
	0x3f W / R TR_SIG_LIM			0x10 Bit7- Bit0 FM Limiting modulation factor		
PHY / DL L	0x40 W / R TxEn			0x03	Bit7	Send synchronization starts to be enabled, 0 To close, 1 To open
			RxEn		Bit6	Receive synchronization starts to be enabled, 0 To close, 1 To open
			MasterMode		Bit5	0 Indicates passive mode, 1 Active mode
			Layer2Slot		Bit4	The bit for mcu provide to HR_C6000 Current time slot usage in Layer 2 mode. Smooth use of time slots when switching from Layer 2 mode to Layer 3. 1 Indicates that the current time slot is used for communication, 0 Indicates that the current time slot is not used for communication.
			CRC_MCU_Control		Bit3	control CRC Verification method, if the bit for 1 ,then CRC The verification process has MCU Handle otherwise HR_C6000 Automatically complete the verification process.
					Bit2	Keep
			Decode_Mode		Bit1-Bit0 Test the error mode. 00 Indicates that the physical layer does not band decode Test mode, 11 Indicates non-test mode communication.	
	0x41 W / R TxNxtSlotEn			0x00	Bit7	The next time slot transmission is enabled. 0 Don't send for the upcoming time slot interruption; 1 Start transmission for the upcoming time slot interruption
			RxNxtSlotEn		Bit6	The reception of the next time slot is enabled. 0 Start not receiving for the upcoming time slot interruption; 1 Start receiving for the upcoming time slot interruption
			SyncFail		Bit5	Out of sync, 0 Indicates that a synchronization signal exists, 1 Indicates that no synchronization information exists, and the physical layer is required to search again.
			begin_v_layer2		Bit4	In Layer 2 mode, the access success flag is written by software 1 After the voice starts to access the voice normally, but the time slot that does not receive voice needs to be bit Zero

			CC_Match_Ctrl		Bit3	Whether receiving and deframing processing is required CC Matching control design, 0 Indicates the need for reception CC Only match will be deframed, 1 No need to receive CC After matching, the deframing process is performed.
					Bit1	Keep
			AutoTest		Bit0	Physical layer testing is enabled, 1 effective
	0x42	R	TransSlot		Bit7	1 Indicates that the current time slot is for transmission, 0 Indicates that the current time slot is not sent
			RecvSlot		Bit6	1 Indicates that the current time slot is for reception, 0 Indicates that the current time slot is not received
			UsedSlot		Bit5	0 Indicates that the current time slot is used for communication, 1 Indicates that the current time slot is not used for communication. HR_C6000 submit to MCU Current time slot usage.
					Bit4-Bit0 Keep	
	0x43	R	RSSILevelH		Bit7-Bit0 RSSI High detection value 8bit	
	0x44	R	RSSILevelL		Bit7-Bit0 RSSI Low detection value 8bit	
	0x45	W / R	Sig_Reduce	0x00	Bit7-Bit0	IQ Mode adjustment IQ Road amplitude; adjust in two-point modulation mode Mod2 Magnitude.
	0x46	W / R	Phase_Reduce	0x00	Bit7-Bit0 Adjust the two-point modulation mode Mod1 Amplitude size	
	0x47	W / R	Two_Point_ Bias	0x00	Bit7-Bit0 Two-point modulation offset adjustment, total 10bit ,its Medium high 2bit Defined in reg0x48 Low 2bit in.	
	0x48	W / R	Two_Point_ Bias	0x00	Bit7	select FSKError Output enable, the bit for 1 , Indicating a register 0x0F Current output value FSKError Statistical value, otherwise EVM Statistics.
					Bit6-Bit2 Keep	
					Bit1-Bit0 Two-point modulation offset adjustment, total 10bit ,its mid Lo 8bit Defined in reg0x47 in.	
	0x49	W	DEV_LIMITERH	0xFF	Bit7-Bit0 Limit the transmission frequency deviation threshold, total 16bit , This register is high 8bit . When sending frequency When it is higher than this value, it will output at this value.	
	0x4A	W	DEV_LIMITERL	0x00	Bit7-Bit0 Limit the transmission frequency deviation threshold, total 16bit , This register is low 8bit . When sending frequency When it is higher than this value, it will output at this value.	
	0x4B	W / R	Code_Type1	0x00	Bit7-Bit6 Custom data type frame (DataType for 1011) Codec type selection: 00 Express BPTC96 Codec; 01 Represents convolution 3/4 Codec; 10 Means no codec;	

						11 Express BPTC72 Codec;
					Bit5-Bit4 Custom data type frame (DataType for	1100) Codec type selection: 00 Express BPTC96 Codec; 01 Represents convolution 3/4 Codec; 10 Means no codec; 11 Express BPTC72 Codec;
					Bit3-Bit2 Custom data type frame (DataType for	1101) Codec type selection: 00 Express BPTC96 Codec; 01 Represents convolution 3/4 Codec; 10 Means no codec; 11 Express BPTC72 Codec;
					Bit1-Bit0 Custom data type frame (DataType for	1110) Codec type selection: 00 Express BPTC96 Codec; 01 Represents convolution 3/4 Codec; 10 Means no codec; 11 Express BPTC72 Codec;
	0x4C W / R	Code_Type2		0x00	Bit7-Bit6 Custom data type frame (DataType for	1111) Codec type selection: 00 Express BPTC96 Codec; 01 Represents convolution 3/4 Codec; 10 Means no codec; 11 Express BPTC72 Codec;
					Bit5-Bit3 Keep	
			data_embrc_ctrl		Bit2	Data control frame EMB Area insertion RC Information selection control, write 0 Means to choose directly from CPU Get, write 1 Indicates that the RC encoding process is performed internally
			data_embrc_en		Bit1	Data Frame SYNC Regional embedding RC Information control is enabled, write 1 Means valid, write 0 Means close
			voice_burstF_emb_ctr		Bit0	voice F Frame embedded information selection, write 0 Directly from CPU Get, write 1 Means internal RC coding
	0x4E R		AD_Bias_I		Bit7-Bit0 AD of I DC input DC bias detection	
	0x4F R		AD_Bias_Q		Bit7-Bit0 AD of Q DC input DC bias detection	
DLL	0x50 W / R	LocalDataType			Bit7-Bit4 Every time slot DataType ,language	sound A ~ F as well as RC Frame type
			LocalVoD		Bit3	0 Means data, 1 Means voice or RC
					Bit2	The location 1 , DataType When data frame header

						Representing data 2 Header, otherwise data header. Not useful for other frame types.
			LocalLCSS		Bit1-Bit0 Every time slot LCSS	
	0x51 R		DLLRecvDataType		Bit7-Bit4 If a data frame is received, it means the received DataType ; If a voice frame is received Bit6-Bit4 Indicates the received voice A , B , C , D , E , F Frame (respectively 123456 Means), Bit7 for 1 .	
			DLLRecvPI		Bit3	Received PI
			DLLRecvCRC		Bit2	The received data verification result, 0 To be correct, 1 Wrong
			SyncClass		Bit1-Bit0	00 Means no sync header, 01 Means voice, 10 Means data, 11 Express RC
	0x52 R		DLLCC		Bit7-Bit4 Received CC	
			CACH		Bit3	The chip receives the acquired AT
					Bit2	The chip receives the acquired TC
					Bit1-Bit0 The chip receives the acquired CACH of LCSS [1: 0]	
	0x52 W		CACH		Bit3	chip BS Downstream transmission configuration word AT
					Bit2	chip BS Downstream transmission configuration word TC
	0x53	R	RC_Info		Bit7-Bit0 RC High information 8bit Or frame F Information super Frame number	
	0x54	R	RC_Info		Bit7-Bit6 Speech frame EMB Regional LCSS information	
					Bit5-Bit3 Keep	
					Bit2-Bit0 RC Low information 3 Bit or frame F Calculation of information law Id	
	0x55	R	Check_sum_reg		Bit7	Keep
					Bit6	CRC8 error flag
					Bit5	gdout check error
					Bit4	qr check error
					Bit3	cs check error
					Bit2	crc16 check error
					Bit1	crc 24 check error
					Bit0	crc 9 check error
	0x5F W / R	Sync_Detect_Ctrl			Bit7-Bit4 Corresponding to four sets of synchronization frame sequence in Layer 2 mode Detectable control enable, 1 Indicates detectable, 0 Indicates that it cannot be detected. Bit7 : MS Bit6 : BS Bit5 : TDMA1 Bit4 : TDMA2	
						Keep
		R	Recv_Sync_Type		Bit1-Bit0 Type of synchronization frame sequence received	

						00 : MS 01 : BS 10 : TDMA1 11 : TDMA2
CCL	0x60		TransControl		Bit7-Bit6	10 Means voice sending request, 01 Represents data sending request
					Bit5-Bit0 Keep	
	0x61		LocalDestAdrressL		0x03 Bit7-Bit0 Local call destination address is low 8Bit	
	0x62		LocalDestAdrressM		0x00 Bit7-Bit0 Local call destination address 8Bit	
	0x63		LocalDestAdrressH		0x00 Bit7-Bit0 Local call destination address is high 8Bit	
Interrupts and data	0x81 W		InterClass1Mask		Bit7-Bit0	0x82 The type of interrupt expressed Mask ,correspond bit for 0 The interrupt is masked.
	0x82 R		InterRequestDeny		Bit7	DMR In mode, it means sending request is rejected; FM In mode, it means sending data request interrupt.
			InterSendStart		Bit6	DMR Under mode 1 Indicates the start of sending; MSK Under mode 1 Indicates that the ping-pong buffer half full interrupt is sent.
			InterSendStop		Bit5	DMR Under mode 1 Indicates the end of sending; MSK Under mode 1 Express PHY The end of transmission is interrupted.
			InterLateEntry		Bit4	DMR Under mode 1 Means after access; MSK Under mode 1 Indicates that the response is interrupted.
			InterRecvData		Bit3	DMR Under mode 1 Indicates the type of received data control frame; MSK Under mode 1 Indicates that the reception was interrupted.
			InterRecvMessage		Bit2	DMR In the mode, it means receiving information; FM Representation in mode FM Function reception detection interrupt.
			InterQuit		Bit1	DMR Abnormal voice exit and interrupt in mode; FM In the mode, it indicates that receiving data is interrupted.
			InterPHYOnly		Bit0	1 Represents the physical layer working alone receiving terminal
	0x83 W		InterClear		Bit7-Bit0 Clear the corresponding interrupt register according to the bit	Device. Bit7: Send request rejected Bit6: Start sending Bit5: End of delivery Bit4: Interruption after voice access Bit3: Data control frame received Bit2: Receive SMS Bit1: Abnormal exit Bit0: The physical layer works alone to receive interrupts

	0x84 R		SendStartVoice		Bit7	Voice transmission
			SendStartCSBK1		Bit6	OACSU Request to send
			KeyUpdateInterp		Bit5	End-to-end voice encryption key update request interrupted
			Over_VocoderRespon		Bit4	AMBE3000 Configuration return interrupt
			SendStartData		Bit3	Data transmission
			SendStartDataPart		Bit2	Partial data retransmission
			SendStartDataFull		Bit1	Retransmit all data
			config_done_pulse		Bit0	Vocoder initialization interrupt
	0x85 W / R SendStartMask				Bit7-Bit0	SendStart Interrupt enable Bit7: Voice start Bit6: Oacsu Request for the first time Bit5: Voice key update interrupted Bit4: VocoderRespon Bit3: Data launch Bit2: Partial data retransmission Bit1: Retransmit all data Bit0: Vocoder initialization interrupt
	0x86 R		Tx_finished		Bit7	Sending complete, including voice and data
			tx_complet_data		Bit6	One without waiting for the confirmation of the feedback packet fragment Send completed
			tx_denied_overtime_o		Bit5	voice OACSU Wait timeout
			rdy_lst_interp		Bit4	Layer 2 mode processing interruption, software configuration information last processing timing control interruption
			tx_complet_confirmed		Bit3	One that needs to wait for the feedback confirmation fragment Send completed
			short_lc_interp		Bit2	ShortLC Receive interrupt
			tx_denied_overtime_bs		Bit1	BS Activation timeout interrupt
			lost_gps_pps		Bit0	GPS Second pulse loss interrupt
	0x87 W / R SendStopMask				Bit7-Bit0	SendStop Interrupt enable Bit7: End of transmission, including data and voice Bit6: One without waiting for the confirmation of the feedback packet fragment Send completed Bit5: Oacsu Request timed out Bit4: Interrupt handling in Layer 2 mode Bit3: One that needs to wait for the feedback confirmation fragment Send completed Bit2: ShortLC Receive interrupt Bit1: BS Activation timeout Bit0: GPS Second pulse loss interrupt
	0x88 R		config_done_auto		Bit7	1 Express DMR The automatic initialization of the vocoder is completed
			config_done_force		Bit6	1 Express DMR The automatic initialization of the vocoder is not completed

			key_update_interp		Bit5	Voice encryption key update interrupted
			emb_update_interp		Bit4	Voice encryption EMB Area update interrupted
			embF_update_interp		Bit3	F frame EMB Message sending interrupted
					Bit2- Bit1 Keep	
			FIFO_FULL		Bit0	MCU write PCM Data give HR_C6000 Of the empty flag bit for 1 At the time fifo Already full. MCU Stop fifo Continue to send data until bit for 0 Only then can the data continue to be sent.
	0x89 W / R		rf_tx_interp_mask		Bit7	Send start RF interrupt mask
			rf_rx_interp_mask		Bit6	End of transmission RF interrupt mask
		R			Bit5- Bit0 Statistics of error codes in synchronization fields	
	0x90 R		RecvDataCRC		Bit7	The entire data reception Fragment of 32bit CRC Verification results, 1 To be correct, 0 Is an error.
					Bit6	Unconfirmed SMS exception error flag. for 1 It means that the corresponding interrupt is an abnormal error of unconfirmed SMS.
					Bit5	FM Under mode FM Function reception detection interrupt
					Bit4	Keep
					Bit3-Bit0 Keep	
	0x98 W / R voice_lostmask				Bit7 ~ Bit5 Speech abnormal interrupt mask	
		R	voice_abnormal_state		Bit2 ~ Bit0 Type of abnormal voice interruption	Bit2 : Time slot 1 Voice statistics voice_sync_lost Abnormal interrupt after time out Bit1 : Time slot 0 Voice statistics voice_sync_lost Abnormal interrupt after time out Bit0 : Abnormal interruption given when the voice reception in Layer 3 mode is out of synchronization
	0x93 R		decode_flag [7: 0]		Bit7- Bit0 5-tone mode: decode_flag [19: 0] for	
	0x94 R		decode_flag [15: 8]		Bit7- Bit0	5-tone Demodulation output;
	0x95 R		decode_flag [19:16]		Bit3- Bit0	2-tone mode: decode_flag [11: 8] for 2-tone Long sound output in decode_flag [7: 0] for 2-tone Two-tone output in CTCSS / CDCSS mode: decode_flag [0] Turn on and enable the speaker; DTMF mode: decode_flag [4] for DTMF Receive the demodulation end status flag; decode_flag [3: 0] for DTMF Decode output;

						XTCSS mode: decode_flag [9] for XTCSS Call sign register; decode_flag [8] for XTCSS Full call sign register; decode_flag [7: 0] for XTCSS Demodulation type flag register.
					Bit7- Bit4 Keep	
MSK Receiving status	0x96 R				Bit7-Bit0 The length of the received data bits.	
	0x97 R				Bit7- Bit6 Keep	
			TrainCodewordFlag		Bit5	0 : Data codeword. 1 : Code word with synchronization sequence.
			TrainErrorBitNum		Bit4- Bit0 Represents the number of error bits in the training sequence (range 0-31) . only in TrainCodewordFlag for 1 Is only valid when it is available.	
FM	0xa0		subvoice_dev_coef	0x0e	Bit7- Bit0	subvoice_dev_coef , Sub-tone modulation frequency deviation
	0xa1 W / R		fm_mod	0x08	Bit7	Reserved, need to be configured as 0
					Bit6	MSK mode
					Bit5	5-Tone
					Bit4	2-Tone
					Bit3	CTCSS
					Bit2	CDCSS
					Bit1	DTMF
					Bit0	XTCSS
	0xa2 W / R	signal_std		0x10	Bit7- Bit6 select XTCSS Send signaling length	
					Bit5- Bit4 Choose whether to send CTCSS Net noise tail, And configure the phase flip angle;	
					Bit3	CDCSS Send phase positive and negative
					Bit2	CDCSS Receiving phase positive and negative
					Bit1	CDCSS Send end code close code enable
					Bit0	Choose whether to send XTCSS End message
	0xa3 W / R		intertone_time	0x05	Bit7- Bit0 2-tone / 5-tone mode: Selcall Adjacent two Frame interval duration (step = 100ms); DTMF mode: DTMF Interval between two adjacent frames (step = 2ms);	
	0xa4 W / R		first_tone_length	0x05	Bit7- Bit0 2-tone mode: 2-tone First tone sent, Receiving time (step = 100ms); 5-tone mode: 5-tone Length of each tone sent and received (step = 100ms); DTMF Mode: Single DTMF Code sending time (step = 2ms);	
	0xa5 W / R		second_tone_length	0x05	Bit7- Bit0 2-tone Second tone sending and receiving time (step = 100ms)	
	0xa6 W / R		long_tone_length	0x0a	Bit7- Bit0 2-tone Long tone demodulation duration	

	0xa7 W / R FREQ_AMP_LIMIT		0x10	Bit7- Bit0 FM Each sub-module receiving frequency energy demodulation gate limit
	0xa8 W / R		0x01	Bit7- Bit0 DTMF mode: DTMF_tone [7: 0] , DTMF sending address; CTCSS mode: ctcss_send_addr , CTCSS sending address.
	0xa9 W / R		0x00	Bit7- Bit0 DTMF mode: DTMF_tone [15: 8] , DTMF sending address; XTCSS mode: xtc_send_hi , XTCSS sending address.
	0xaa W / R		0x00	Bit7- Bit0 DTMF mode: DTMF_tone [23:16] , DTMF sending address; XTCSS mode: xtc_send_low , XTCSS Type of delivery.
	0xab W / R		0x00	Bit7- Bit0 DTMF mode: DTMF_tone [31:24] , DTMF sending address; CDCSS mode: dcs_code [7: 0] , CDCSS Send code low 8 Bit.
	0xac W / R		0x00	Bit7- Bit0 DTMF mode: DTMF_tone [39:32] , DTMF sending address; CDCSS mode: dcs_code [8] , CDCSS Send the highest bit of the code, Bit0 Said.
	0xad W / R		0x00	Bit7- Bit0 DTMF mode: DTMF_tone [47:40] , DTMF sending address; 2-Tone / 5-Tone mode: selcall_tone [7: 0] , Selcall-tone sending address.
	0xae W / R			Bit7- Bit0 DTMF mode: DTMF_tone [55:48] , DTMF sending address; 2-Tone / 5-Tone mode: selcall_tone [15: 8] , Selcall-tone sending address.
	0xaf W / R		0x00	Bit7- Bit0 DTMF mode: DTMF_tone [63:56] , DTMF sending address; 2-Tone / 5-Tone mode: selcall_tone [19:16] , Selcall-tone sending address, Bit3-Bit0 .
Other configuration	0xb0 W / R Ambe1000_noise_reg0		0xCE Bit7- Bit0	Configuration AMBE1000 Squelch output control Packaged 9 Pc byte parameter.
	0xb1 W / R Ambe1000_noise_reg1		0xC9 Bit7- Bit0	
	0xb2 W / R Ambe1000_noise_reg2		0x32 Bit7- Bit0	
	0xb3 W / R Ambe1000_noise_reg3		0xE8 Bit7- Bit0	
	0xb4 W / R Ambe1000_noise_reg4		0xA4 Bit7- Bit0	
	0xb5 W / R Ambe1000_noise_reg5		0x06 Bit7- Bit0	

	0xb6 W / R Ambe1000_noise_reg6		0x2C Bit7- Bit0		
	0xb7 W / R Ambe1000_noise_reg7		0xF7 Bit7- Bit0		
	0xb8 W / R Ambe1000_noise_reg8		0xB4 Bit7- Bit0		
Clock configuration	0xb9 W / R Sys_clk_Reg		0x05 Bit7- Bit0 Configure the system clock frequency		
	0xba W / R Codec_clk_Reg		0x04 Bit7- Bit0 Configure built-in codec Working clock frequency		
	0xbb W / R ClkOut_Reg		0x02 Bit7- Bit0 Configure the output clock operating frequency		
	0xc0 W / R	rf_pre_on_rx	0x00 Bit7- Bit6 Keep		
				Bit5- Bit0 The RF transmitter can be switched to the receiving interruption position in advan	
				Match, increasing step size is about 100μs .	
	0xc1 W / R RF_LEVEL		0x00 Bit7		RF_LEVEL Control selection, 0 It is generated by the chip, 1
					Expressed by MCU External configuration write
				Bit6	external MCU Configured RF_LEVEL value
				Bit5	In three-tier mode 30ms Time slot interrupt open enable
				Bit4- Bit0 Keep	
	0xc2 W / R Codec_AGC_CTRL		0x00 Bit7		Codec of mic Gain AGC Control enabled,
					1 Means open, 0 Means close
				Bit6- Bit0 Keep	
	0xc3 W / R CODEC_OPTIMALH		0x08 Bit7- Bit0 Codec High output optimal amplitude value 8 Bit		
					take Codec High average output amplitude 8 Bit
	0xc4 W / R CODEC_OPTIMALL		0x00 Bit7- Bit0 Codec Low output optimal amplitude value 8 Bit		
					take Codec Low average output amplitude 8 Bit
	0xc5 W / R CODEC_LOWLEVELH 0x00 Bit7- Bit0 Codec Highest output amplitude value 8 Bit				
	0xc6 W / R CODEC_LOWLEVELL		0x64 Bit7- Bit0 Codec Highest output amplitude value 8 Bit		
	0xc7 W/R RF_3TC_ON		0x00 Bit7		管脚复用控制
				Bit6	1 表示 RF_3TC 开启在 30ms 时隙 边界之后； 0 表示 RF_3TC 开启在 30ms 时隙边界之前；
				Bit5- Bit0 根据 Bit6 定义，相对 30ms 边界的	
				提前或延时的时间量设置，递增步 长为约 100μs	
				。	
	0xc8 W/R RF_3TC_OFF		0x00 Bit7		保留
				Bit6	1 表示 RF_3TC 关闭在 30ms 时隙 边界之后； 0 表示 RF_3TC 关闭在 30ms 时隙边界之前；
				Bit5- Bit0 根据 Bit6 定义，相对 30ms 边界的	
				提前或延时的时间量设置，递增步 长为约 100μs	
				。	
	0xc9 W/R RF_5TC_ON		0x00 Bit7		管脚复用控制
				Bit6	1 表示 RF_5TC 开启在 30ms 时隙 边界之后； 0 表示 RF_5TC 开启在 30ms 时隙边界之前；

					Bit5- Bit0 根据 Bit6 定义，相对 30ms 边界的提前或延时的时间量设置，递增步 长为约 100μs 。
	0xca W/R RF_5TC_ OFF			0x00 Bit7		保留
					Bit6	1 表示 RF_5TC 关闭在 30ms 时隙 边界之后；0 表示 RF_5TC 关闭在 30ms 时隙边界之前；
					Bit5- Bit0 根据 Bit6 定义，相对 30ms 边界的提前或延时的时间量设置，递增步 长为约 100μs 。
	0xcb W/R RF_ANT_ON			0x00 Bit7		管脚复用控制
					Bit6	1 表示 RF_ANT 开启在 30ms 时隙 边界之后；0 表示 RF_ANT 开启在 30ms 时隙边界之前；
					Bit5- Bit0 根据 Bit6 定义，相对 30ms 边界的提前或延时的时间量设置，递增步 长为约 100μs 。
	0xcc W/R RF_ANT_OFF			0x00 Bit7		保留
					Bit6	1 表示 RF_ANT 关闭在 30ms 时隙 边界之后；0 表示 RF_ANT 关闭在 30ms 时隙边界之前；
					Bit5- Bit0 根据 Bit6 定义，相对 30ms 边界的提前或延时的时间量设置，递增步 长为约 100μs 。
	0xcd W/R RF_3RC_ON			0x00 Bit7		管脚复用控制
					Bit6	1 表示 RF_3RC 开启在 30ms 时隙 边界之后；0 表示 RF_3RC 开启在 30ms 时隙边界之前；
					Bit5- Bit0 时间量设置，递增步长为约 100μs 。	
	0xce W/R RF_3RC_OFF			0x00 Bit7		保留
					Bit6	1 表示 RF_3RC 关闭在 30ms 时隙 边界之后；0 表示 RF_3RC 关闭在 30ms 时隙边界之前；
					Bit5- Bit0 根据 Bit6 定义，相对 30ms 边界的提前或延时的时间量设置，递增步 长为约 100μs 。
	0xcf W/R RF_5RC_ON			0x00 Bit7		管脚复用控制
					Bit6	1 表示 RF_5RC 开启在 30ms 时隙 边界之后；0 表示 RF_5RC 开启在 30ms 时隙边界之前；
					Bit5- Bit0 时间量设置，递增步长为约 100μs 。	
	0xd0 W/R RF_5RC_OFF			0x00 Bit7		保留
					Bit6	1 表示 RF_5RC 关闭在 30ms 时隙

						边界之后； 0 表示 RF_5RC 关闭在 30ms 时隙边界之前；
					Bit5- Bit0 根据 Bit6 定义，相对 30ms 边界的	提前或延时的时间量设置，递增步 长为约 100μs 。
FM 亚音 控制	0xd1 W/R	dtmf_code_width		0x04	Bit7- Bit5 保留	
					Bit4- Bit0 DTMF 发送帧数标志位	
	0xd2 W/R			0xd0 Bit7- Bit0		sample_size[7:0] ， FM 各子模块采 样深度
	0xd3 W/R			0x07 Bit7- Bit5 保留		
					Bit4	CDCSS 接收地址的最高位
					Bit3- Bit0	sample_size[11:8] ， FM 各子模块采 样深度
	0xd4 W/R			0x01 Bit7- Bit0 CTCSS 模式： CTCSS 接收地址		CDCSS 模式： CDCSS 接收地址低 8 位 XTCSS 模式： XTCSS 接收地址
MSK 模 式	0xd5 W/R	AcqEnable		0x00 Bit7		1 ： PHY 进行捕获操作。 0 ：不起作用。 注：此信息为上跳变起作用，因此 PHY 读到 AcqEnable 被 MAC 置 1 之后，立即清 0 。
			OperationType		Bit6	0 ：表示空闲状态。 1 ：表示工作状态。
			ChannelType		Bit5- Bit4 00 ：	控制信道。 01 ：业务信道。 10 ：数据信道。 11 ：保留。
			TranOrRecFlag		Bit3	0 ：接收。 1 ：发送。
			SoftReset		Bit2	0 ：不起作用。 1 ：复位。
					Bit1- Bit0 保留	
	0xd6 W/R			0x00 Bit7- Bit6 保留		
			RemBitNum		Bit5- Bit0 MAC	剩余没有发的 Bit 位。范围 0-63 。
	0xd7 W/R	MultiMessageTransFlag		0x00 Bit7		0 ：不起作用 1 ：当前码字发完之后，要添加翻 转比特位。 注：此信息为上跳变起作用，因此

						PHY 读到 AcqEnable 被 MAC 置 1 之后，立即清 0 。并且只对 PHY 组帧有效。
			RxInterMask		Bit6	0: 不起作用。 1: 接收中断屏蔽。
			CtrlDataInterMask		Bit5	0: 不起作用。 1: 接收中断屏蔽。
			MacFrameEn		Bit4	0 ： PHY 组帧。 1 ： MAC 组帧。
			MACTransFinishFlag		Bit3	0 ：不起作用。 1 ：对 PHY 组帧来说当前码字取完 毕之后结束取比特数据。对 MAC 组帧来说当前码字取完并且再取 RemBitNum 长度之后结束取比特 数据。
			Unsolicited		Bit2	0 ：发送响应信息。 1 ：主动发送信息。
			msk_voice_send_en		Bit1	0 ：发送 MSK 信令信息。 1 ：发送 FM 语音。
					Bit0	保留
	0xdc		TDMA_Slot_Num_H		Bit0	集群模式下从 short_lc 信息中获取 的复帧号
	0xdd		TDMA_Slot_Num_L		Bit7- Bit0	
内 置 codec 参数配置	0xe0 W/R				Bit7	Codec 配置控制使能。置 1 时候，CPU 通过寄存器配置控制 Codec 开关；置 0 时候， HR_C6000 自动 控制 Codec 的开关。
					Bit6	Linein1 使能控制， 1 开启。
					Bit5	Linein2 使能控制， 1 开启。
					Bit4	LineOut1 使能控制， 1 开启。
					Bit3	LineOut2 使能控制， 1 开启。
					Bit2	Mic_n 使能控制， 1 开启；
					Bit1	Mic_p 使能控制， 1 开启；
					Bit0	I2S 模式选择， HR_C6000 工作在 Slave 模式，应配置为 1 。
	0xe2 W/R				Bit7	Default 0
					Bit6	DAC 开关使能，正常工作模式为 0 。
					Bit5	Codec 偏置开关使能，正常工作模 式为 0 ；配置为 1 后， Codec 的 DAC 和 ADC 均不能正常工作。在待机 模式下，该值为 1.
					Bit4	Codec 的 ADC 使能开关，正常工 作模式为 0 ， ADC 不工作时候需

						要配置成 1 ；
					Bit3	Codec 的 ADC 端 Mic 放大模块使 能，正常工作模式为 0 ， ADC 不 工作时候需要配置成 1。
					Bit2	抗 POP 噪音使能，需要在 DAC 正 常工作 1ms 后配置成 1 ，在关闭前 10ms 配置成 0 。
					Bit1	DAC 输出到功放前的开关，正常 工作模式配置为 1 ；配置成 0 则 DAC 无法输出到 LineOut 。
					Bit0	Codec 的 PowerDown 控制，正常 工作模式下配置为 0 ；待机时候为 1 。
	0xe3 W/R				Bit7- Bit6 Default 01	
					Bit5- Bit4 Default 01	
					Bit3- Bit1 Default 001 Bit0	
						Codec 内部 DAC 和 ADC 直通使 能，置 1 时使能有效，正常工作时 候配置为 0 。
	0xe4 W/R				Bit7-Bit6 Lineout 输出增益。其中 00 对应 0dB ； 01 对应 2dB ； 10 对应 4dB ； 11 对应 6dB 。	
					Bit5-Bit4 Mic 第一级增益。 00 对应 0dB ； 01 对应- 6dB ；其他对应- 12dB	
					Bit3-Bit0 Mic 第二级增益，在第一级增益的基础上按照 3dB 阶梯递增。其中 0000 最小。	
	0xe5 W/R				Bit7-Bit1 Default: 00001010	
	0xe6 W/R				Bit7	HP_PREV_EN ，默认为 0
					Bit6-Bit5 HP_TIME_SET ，默认为 00 Bit4	
						POP_SEL_EN ，默认为 0
					Bit3-Bit0 保留	

附属参数配置表

类型 地址		名称	缺省值	定义	说明
DATA SYNC	0x04	DATA SYNC1	0xdf	Bit7-Bit0 发送数据同步字	
	0x05	DATA SYNC2	0xf5	Bit7-Bit0	段 48bit
	0x06	DATA SYNC3	0x7d	Bit7-Bit0	
	0x07	DATA SYNC4	0x75	Bit7-Bit0	
	0x08	DATA SYNC5	0xdf	Bit7-Bit0	
	0x09	DATA SYNC6	0x5d	Bit7-Bit0	
RC SYNC	0x0a	RC SYNC1	0xdf	Bit7-Bit0 发送 RC 同步字段	
	0x0b	RC SYNC2	0xf5	Bit7-Bit0	48bit

	0x0c	RC SYNC3	0x7d	Bit7-Bit0	
	0x0d	RC SYNC4	0x75	Bit7-Bit0	
	0x0e	RC SYNC5	0xdf	Bit7-Bit0	
	0x0f	RC SYNC6	0x5d	Bit7-Bit0	
	0x24	scramble_reg0	0x00	Bit7-Bit0	语音加密初始化
	0x25	scramble_reg1	0x00	Bit7-Bit0	寄存器
	0x26	dscramble_reg0	0x00	Bit7-Bit0	语音解密初始化
	0x27	dscramble_reg1	0x00	Bit7-Bit0	寄存器
	0x2A	RS_H_INITREG0	0x00	Bit7-Bit0	语音帧头 RS 校验
	0x2B	RS_H_INITREG1	0x00	Bit7-Bit0	初值
	0x2C	RS_H_INITREG2	0x00	Bit7-Bit0	
	0x2D	RS_T_INITREG0	0x00	Bit7-Bit0	帧尾 RS 校验初值
	0x2E	RS_T_INITREG1	0x00	Bit7-Bit0	
	0x2F	RS_T_INITREG2	0x00	Bit7-Bit0	
	0x30	CSBK_INITREG0	0x00	Bit7-Bit0	CSBK 包 CRC16 校 验初值
	0x31	CSBK_INITREG1	0x00	Bit7-Bit0	
	0x3A	DATAH_INITREG0	0x00	Bit7-Bit0	数据帧头 CRC16
	0x3B	DATAH_INITREG1	0x00	Bit7-Bit0	校验初值
	0x3C	PI_INITREG0	0x00	Bit7-Bit0	PI 帧 CRC16 校验 初值
	0x3D	PI_INITREG1	0x00	Bit7-Bit0	
	0x3E	MBC_INITREG0	0x00	Bit7-Bit0	MBC 帧 CRC16 校
	0x3F	MBC_INITREG1	0x00	Bit7-Bit0	验初值
	0x40	CRC8_INITREG	0x00	Bit7-Bit0	CRC8 校验初值
MS DATA SYNC	0x47	DATA SYNC1	0xd5	Bit7-Bit0	接收 MS 数据同步
	0x48	DATA SYNC2	0xd7	Bit7-Bit0	字段 48bit
	0x49	DATA SYNC3	0xf7	Bit7-Bit0	
	0x4a	DATA SYNC4	0x7f	Bit7-Bit0	
	0x4b	DATA SYNC5	0xd7	Bit7-Bit0	
	0x4c	DATA SYNC6	0x57	Bit7-Bit0	
	0x4d	CRC9_INITREG0	0x00	Bit7-Bit0	各速率确认短信
	0x4e	CRC9_INITREG1	0x00	Bit7-Bit0	CRC9 校验初值
	0x4f	CRC9_INITREG2	0x00	Bit7-Bit0	
	0x50	CRC9_INITREG3	0x00	Bit7-Bit0	
	0x52	RSSIBottonH	0x1a	Bit7-Bit0	DMR 模式下，信 号检测阈值高 8 位
	0x53	RSSIBottonL	0xf0	Bit7-Bit0	DMR 模式下，信 号检测阈值低 8 位
	0x54	MaxValue	0x78	Bit7-Bit0	同步帧检测阈值
	0x55	Sig_COR_VALUE	0x67	Bit7-Bit0	信号到达检测阈 值
BS DATA SYNC	0x56	DATA SYNC1_1	0xdf	Bit7-Bit0	接收 BS 数据同步
	0x57	DATA SYNC2_1	0xf5	Bit7-Bit0	字段 48bit
	0x58	DATA SYNC3_1	0x7d	Bit7-Bit0	

	0x59 DATA SYNC4_1	0x75	Bit7-Bit0	
	0x5a DATA SYNC5_1	0xdf	Bit7-Bit0	
	0x5b DATA SYNC6_1	0x5d	Bit7-Bit0	
	0x5c CRC32_INITREG0	0x00	Bit7-Bit0	CRC32 校验计算 初值
	0x5d CRC32_INITREG1	0x00	Bit7-Bit0	
	0x5e CRC32_INITREG2	0x00	Bit7-Bit0	
	0x5f CRC32_INITREG3	0x00	Bit7-Bit0	
多组呼 地址	0x60 GroupAddr_L1		Bit7-Bit0 第 1 组 24bit 组呼	
	0x61 GroupAddr_M1		Bit7-Bit0	地址
	0x62 GroupAddr_H1		Bit7-Bit0	
	……		……	
	0xbd GroupAddr_L32		Bit7-Bit0 第 32 组 24bit 组呼	
	0xbe GroupAddr_M32		Bit7-Bit0	地址
	0xbf GroupAddr_H32		Bit7-Bit0	
MSK 模式	0x12a TrainErrorThreshold		Bit7-Bit6 保留	
			Bit5-Bit0 捕获和同步时的	训练序列判决门 限。
	0x12b DTBeforeTransAndRec			接收脉冲和发射 起始脉冲之间的 延迟。这里配置的 值是以 19.2kHz 采 样时钟为基值假 设配置值为 n ，则 延迟时间为 n/19.2 毫秒。
	0x12c NT			MAC 组帧到空口 发送起点的时延 差值
	0x12d ChannelDelay			业务信道上 TSC 响应手台主动消 息的最大延迟（单 位比特）。
RC SYNC	0x12e RC SYNC1	0x77	Bit7-Bit0 接收 RC 同步字段	
	0x12f RC SYNC2	0xd5	Bit7-Bit0	48bit
	0x130 RC SYNC3	0x5f	Bit7-Bit0	
	0x131 RC SYNC4	0x7d	Bit7-Bit0	
	0x132 RC SYNC5	0xfd	Bit7-Bit0	
	0x133 RC SYNC6	0x77	Bit7-Bit0	
TDMA1 SYNC	0x134 DATA SYNC1_2	0xf7	Bit7-Bit0 接收 TDMA1 数据	
	0x135 DATA SYNC2_2	0xfd	Bit7-Bit0	同步字段 48bit
	0x136 DATA SYNC3_2	0xd5	Bit7-Bit0	
	0x137 DATA SYNC4_2	0xdd	Bit7-Bit0	

	0x138	DATA SYNC5_2	0xfd	Bit7-Bit0	
	0x139	DATA SYNC6_2	0x55	Bit7-Bit0	
TDMA2 SYNC	0x13a	DATA SYNC1_3	0xd7	Bit7-Bit0 接收 TDMA2 数据	
	0x13b	DATA SYNC2_3	0x55	Bit7-Bit0	同步字段 48bit
	0x13c	DATA SYNC3_3	0x7f	Bit7-Bit0	
	0x13d	DATA SYNC4_3	0x5f	Bit7-Bit0	
	0x13e	DATA SYNC5_3	0xf7	Bit7-Bit0	
	0x13f	DATA SYNC6_3	0xf5	Bit7-Bit0	

附录 ：

A FM 通路具体使用说明

A1 提示音通路

A1.1 参数配置

- 提示音主要包括开机铃声，来电、来信铃声等。
- 配置 0x06[2] ，选择内置或外置 Codec 。
- 当使用外置 Codec 时，需要配置 0x36[7] = 0 ，用于开启与外置 Codec I2S 接口相连 的 BCLK 、 LRCK 信号；配置寄存器 0x30 、 0x31 用于 BCLK 频率的确定，配置寄 存器 0x32 、 0x33 用于 LRCK 频率的确定，具体确定方法见外置 Codec I2S 接口读 写时序。
- 当使用内置 Codec 时，配置寄存器 0x0D = 0x10 ，内置 Codec 在正常工作模式并且 由系统自动控制其 AD/DA 开关，当内置 Codec 不工作时可以通过修改该寄存器配 置进入低功耗状态；配置寄存器 0x0E = 0x8E ，开启 MicEn 、 HPoutEn 、 LineoutEn ， 默认 HPoutVol 为 0db ，可以根据实际调节；配置寄存器 0x0F = 0xB8 ，默认 ADLinVol 与 MicVol 为 0dB ，可以根据实际调节；配置寄存器 0x38 = 0x00 ，不做任何修改。
- 配置寄存器 0x37 = 0x00 ，不改变 DACDATA 的大小。
- 配置 0x06[1] = 1 ，开启提示音通路。
- 此后需立即通过操作 U_SPI 接口写数据给 Codec 实现提示音放音。
- 提示音结束，需立即配置 0x06[1] = 0 ，关闭提示音通路。

A1.2 使用说明

通过操作 U_SPI 接口，写数据给 Codec ，实现提示音的放音。

U_SPI 接口帧格式与要求

图 A.1 提示音操作 U_SPI 接口帧格式

其中： Cmd=8'h03 ， Addr=8'h00 ，由于一个 DACDATA 为 16bits ，所以需要 64 个 8bits DATA 。

提示音通路内部缓存深度为 64 ，通过 MCU 操作提示音通路为：首先打开提示音通路， 然后每 1ms MCU 读取寄存器 0x88[0] ，当寄存器值为 0 时， MCU 通过 U_SPI 连续写 32 个 DACDATA 给 HR_C6000 ，提示音结束关闭此通路。

A2 模拟通路

A2.1 参数配置

- 配置 0x06[1] = 0 ， 0x10[7] = 1 ，关闭提示音通路，开启 FM 通路；
- 配置 0x06[2] ，选择内置或外置 Codec 。
- 选择内置或者外置 Codec 后，需要对内置或者外置 Codec 相关寄存器做进一步配 置，具体见提示音通路。

- 配置寄存器 0x37 = 0x00 ，不改变 DACDATA 的大小。

A2.2 使用说明

A2.2.1 CTCSS

- 配置 0xa1[7:0] = 8'h08 进入 CTCSS 模式；

A2.2.1.1 参数配置与初始化

- 配置 0xa0[7:0] = 8'h0d ，设置 CTCSS 亚音发送调制频偏为 350Hz ；
- 配置 0xa2[5:4] = 2'b01 （默认），设置 CTCSS 尾音消除相位翻转的类型； 其中： 00 表示尾音消除功能关； 01 表示标准相位翻转（ 240 度）；
  10 表示非标准相位翻转(180 度)
- 配置 0xa7[7:0] = 8'h10 ，设置 CTCSS 亚音检测门限;
- 配置 0xa8[7:0] = 8'h04 ，设置 CTCSS 亚音发送频率;
  CTCSS 一共包含有 51 组模拟亚音频率，范围从 62.5~254.1Hz ，如下表所示：

	1	2	3	4	5	6	7
亚音频率（Hz）	67	71.9	74.4 77		79.7	82.5	85.4
	8	9	10	11	12	13	14
亚音频率（Hz） 88.5		91.5	94.8	97.4 100		103.5 107.2	
	15	16	17	18	19	20	21
亚音频率（Hz） 110.9	114.8 118.8			123	127.3	131.8 136.5	
	22	23	24	25	26	27	28
亚音频率（Hz） 141.3	146.2 151.4	156.7 162.2				167.9 173.8	
	29	30	31	32	33	34	35
亚音频率（Hz） 179.9	186.2 192.8	203.5 210.7				218.1 225.7	
	36	37	38	39	40	41	42
亚音频率（Hz） 233.6	241.8 250.3			69.3	62.5	159.8 165.5	

	43	44	45	46	47	48	49
亚音频率（Hz）	171.3	177.3	183.5	189.9	196.6	199.5	206.5
	50	51					
亚音频率（Hz）	229.1	254.1					

- 配置 0xd3[7:0] = 8'h07 ， 0xd2[7:0] = 8'hd0 ，设置 CTCSS 解调采样深度，默认为 2000（ 8KHz ， 250ms ）；
- 配置 0xd4[7:0] = 8'h04 ，设置 CTCSS 接收频率，与上表相对应；

A2.2.1.2 发送与接收

- 发送：当 PTT 按键按下后，系统判断当前状态是否处于 CTCSS 模式（ 0xa1[7:0] = 8'h08 ），如果是，则将调制频偏为 350Hz 的亚音信号加载在语音上一同输出。 在 PTT 释放的时刻，如果开启了尾音消除功能，则经过相位翻转后的亚音信号将 继续发送大约 155ms ；

- 接收： CTCSS 接收模式下，系统解调空中信号亚音频率，如果与预设的地址相匹 配，则寄存器 0x93[0] 将被自动置高； MCU 在接收到 FM 中断后，判断该 bit 的状 态选择开启（ 0x36[7:0] = 8'h72 ）或者关闭扬声器（ 0x36[7:0] = 8'h80 ）；

A2.2.2 **CDCSS**

- 配置 0xa1[7:0] = 8'h04 进入 CDCSS 模式；

A2.2.2.1 参数配置与初始化

- 配置 0xa0[7:0] = 8'h03 ，设置 CDCSS 亚音发送调制频偏为 350Hz ；
- 配置 0xa2[3:1] = 3'b001 （默认），设置 CDCSS 信号标准；
  0xa2[3] ：“ 1 ”为 CDCSS 发送相位反，“ 0 ”为正；
  0xa2[2] ：“ 1 ”为 CDCSS 接收相位反，“ 0 ”为正；
  0xa2[2] ：“ 1 ”为 CDCSS 发送尾音关闭码功能开启；
  “ 0 ”为发送尾音关闭码功能关闭；
- 配置 0xac[0]=0 ， 0xab[7:0] = 8'h4c ，设置 CDCSS 发送码“ 114 ”；
- 配置 0xd3[3:0] = 4'h3 ， 0xd2[7:0] = 8'h20 ，设置 CDCSS 解调采样深度，默认为 800（ 8KHz ， 100ms ）；
- 配置 0xd3[4]=0 ， 0xd4[7:0] = 8'h4c ，设置 CDCSS 接收码“ 114 ”；
- 配置 0x104[7:0]= 8'h7f ， 0x103[7:0]= 8'h49 ， 0x102[7:0]= 8'h9d ，设置 CDCSS 尾音 关闭码检测解调系数。默认为 24bit 的十进制数 8341917 ，对应的检测频率为 134.4Hz 单音（标准）。 由公式： 2*COS(2*π*134.4Hz/8000Hz 采样时钟)经过 2^22 量化后得 到；

A2.2.2.2 发送与接收

- 发送： PTT 有效时，调制频偏为 350Hz 的 CDCSS 信号伴随语音信号一同发送，在 PTT 释放时，如果尾音关闭码功能开启，则继续发送一段频率为 134.4Hz 的单音， 反之则发送结束；

- 接收： CDCSS 检测到与接收地址相匹配的 CDCSS 码时，则寄存器 0x93[0] 将被自 动置高； MCU 在接收到 FM 中断后，判断该 bit 的状态选择开启（ 0x36[7:0] = 8'h72 ）

或者关闭扬声器（ 0x36[7:0] = 8'h80 ），此处操作与 CTCSS 相同；

A2.2.3 **DTMF**

- 配置 0xa1[7:0] = 8'h02 进入 DTMF 模式；

A2.2.3.1 参数配置与初始化

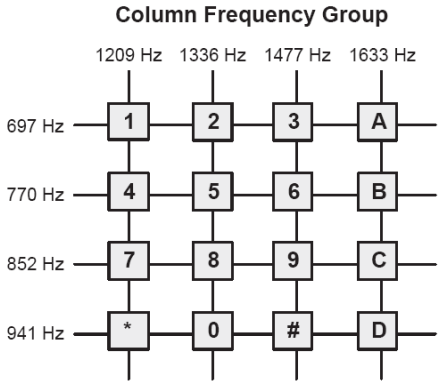
- 配置 0xa0[7:0] = 8'h39 ，设置 DTMF 发送调制频偏为 1.8KHz ；
- 配置 0xa4[7:0] = 8'h32 ，设置 DTMF 信号单次发送时长，默认 100ms ，可调节的步 进长度为 2ms ；
- 配置 0xa3[7:0] = 8'h19 ，设置 DTMF 相邻帧间隙时长，默认 50ms ，可调节的步进 长度为 2ms ；
- 配置 0xa7[7:0] = 8'h0a ，设置 DTMF 解调门限；
- 配置 0xaf ， 0xae ， 0xad ， 0xac ， 0xab ， 0xaa ， 0xa9 ， 0xa8 ，设置 DTMF 发送码（最 高支持 16 位）。自高向低配置，例如配置“ 1234 ”，则为 0xaf = 8'h12 ， 0xae = 8'h34 ；
- 配置 0xd1[4:0] = 5'b00100 ，设置 DTMF 发送帧长，例如 DTMF 码“ 1234 ”的发送 帧长为 4 ；
- 配置 0xd3[3:0] = 4'h4 ， 0xd2[7:0] = 8'h20 ，设置 DTMF 解调采样深度，默认为 1056（ 32KHz ， 33ms ）；
- 接收解调系数配置： 配置{ 0x104 ， 0x103 ， 0x102}=24'h7ecd9d（频率 697Hz 对应解调值）； 配置{ 0x107 ， 0x106 ， 0x105}=24'h7e8a34（频率 770Hz 对应解调值）； 配置{ 0x10a ， 0x109 ， 0x108}=24'h7e368c（频率 852Hz 对应解调值）； 配置{ 0x10d ， 0x10c ， 0x10b}=24'h7dd245（频率 941Hz 对应解调值）； 配置{ 0x110 ， 0x10f ， 0x10e}=24'h7c690d（频率 1209Hz 对应解调值）； 配置{ 0x113 ， 0x112 ， 0x111}=24'h7b9f03（频率 1336Hz 对应解调值）； 配置{ 0x116 ， 0x115 ， 0x114}=24'h7aa7a8（频率 1477Hz 对应解调值）； 配置{ 0x119 ， 0x118 ， 0x117}=24'h7979f5（频率 1633Hz 对应解调值）；

  由公式： 2*COS(2*π* 待检测频率/ 32000Hz 采样时钟)经过 2^22 量化后得到；

- 发送频率配置： 配置{ 0x11b ， 0x11a}=16'h0593 （频率 697Hz 对应相位值）； 配置{ 0x11d ， 0x11c}=16'h0629 （频率 770Hz 对应相位值）； 配置{ 0x11f ， 0x11e}=16'h06d1（频率 852Hz 对应相位值）； 配置{ 0x121 ， 0x120}=16'h0787 （频率 941Hz 对应相位值）； 配置{ 0x123 ， 0x122}=16'h09ac （频率 1209Hz 对应相位值）； 配置{ 0x125 ， 0x124}=16'h0ab0 （频率 1336Hz 对应相位值）； 配置{ 0x127 ， 0x126}=16'h0bd1（频率 1477Hz 对应相位值）； 配置{ 0x129 ， 0x128}=16'h0d10 （频率 1633Hz 对应相位值）；

  由公式：(待发送频率/ 32000Hz 采样时钟)经过 2^16 量化后得到。

  DTMF 码与频率对应关系如下表所示：



A2.2.3.2 发送与接收

- 发送： PTT 有效时，系统将保存在寄存器 0xaf ~ 0xa8 中的 DTMF 码发送，发送帧 长由 0xd1[4:0] 中指定， DTMF 均为 single 模式，即每次只发送一遍序列码，下次 发送需等到新的 PTT 有效；

- 接收： MCU 在每次 FM 中断来临时将寄存器 0x93[3:0] 中的数据保存在一个队列空 间，当检测到 0x93[4] = 1 时，将队列中的信息与软件提前配置的 DTMF 接收地址 比较，如果匹配则打开语音通路（ 0x36[7:0] = 8'h72 ），反之则关闭扬声器（ 0x36[7:0] = 8'h80 ）。

A2.2.4 Selcall-tone （ **2-tone** ）

- 配置 0xa1[7:0] = 8'h10 进入 2-tone 模式；

A2.2.4.1 参数配置与初始化

- 配置 0xa0[7:0] = 8'h39 ，设置 2-tone 发送调制频偏为 1.8KHz ；
- 配置 0xa4[7:0] = 8'h05 ，设置 2-tone 第一音发送时长，默认 500ms ，可调节的步进 长度为 100ms ；
- 配置 0xa3[7:0] = 8'h05 ，设置 2-tone 相邻帧间隙时长，默认 500ms ，可调节的步进 长度为 100ms ；
- 配置 0xa5[7:0] = 8'h05 ，设置 2-tone 第二音发送时长，默认 500ms ，可调节的步进 长度为 100ms ；
- 配置 0xa6[7:0] = 8'h0a ，设置 2-tone 的长音发送时长，默认 1000ms ，可调节的步进 长度为 100ms ；
- 配置 0xa7[7:0] = 8'h0a ，设置 2-tone 解调门限；
- 配置{ 0xaf[3:0], 0xae[7:4] } ，设置 2-tone 发送码，由“ A ”、“ B ”、“ C ”、“ D ”两两 配对组成或者单独输出作为长音 ，例如“ A-B ”或者“ long A ”；
- 配置 0xd3[3:0] = 4'hc ， 0xd2[7:0] = 8'h80 ，设置 2-tone 解调采样深度，默认为 3200 （ 32KHz ， 100ms ）；
- 接收解调系数配置： 配置{ 0x104 ， 0x103 ， 0x102}=24'h767041 (A 音 1981Hz 对应解调值)； 配置{ 0x107 ， 0x106 ， 0x105}=24'h7ce537 (B 音 1124Hz 对应解调值)； 配置{ 0x10a ， 0x109 ， 0x108}=24'h7c7b1e (C 音 1197Hz 对应解调值)； 配置{ 0x10d ， 0x10c ， 0x10b}=24'h7c0285 (D 音 1275Hz 对应解调值)；

配置{ 0x110 ， 0x10f ， 0x10e}=24'h7b7a03 (E 音 1358Hz 对应解调值)；

由公式： 2*COS(2*π* 待检测频率/ 32000Hz 采样时钟)经过 2^22 量化后得到；

- 发送频率配置： 配置{ 0x11b ， 0x11a}=16'h0fd9 （ A 音 1981Hz 对应相位值)； 配置{ 0x11d ， 0x11c}=16'h08fe （ B 音 1124Hz 对应相位值)； 配置{ 0x11f ， 0x11e}=16'h0993 （ C 音 1197Hz 对应相位值)； 配置{ 0x121 ， 0x120}=16'h0a33 （ D 音 1275Hz 对应相位值)； 配置{ 0x123 ， 0x122}=16'h0add （ E 音 1358Hz 对应相位值)；

由公式：(待发送频率/ 32000Hz 采样时钟)经过 2^16 量化后得到。

2-tone 码与频率对应关系默认采用 CCIR1 标准。

A2.2.4.2 发送与接收

- 发送： PTT 有效时，系统将保存在寄存器 0xaf[3:0], 0xae[7:4] 中的 2-tone 码发送， 发送格式由 0xa3 ~ 0xa6 指定， 2-tone 均为 single 模式，即每次只发送一遍序列码， 下次发送需等到新的 PTT 有效；

- 接收： MCU 在每次 FM 中断来临时将寄存器 0x93 中的数据与软件预设的两音接收 地址比较，将寄存器 0x94[3:0] 中的数据与软件预设的长音接收地址比较，如果其 中有一种匹配，则打开扬声器通路（ 0x36[7:0] = 8'h72 ），反之则关闭扬声器（ 0x36[7:0] = 8'h80 ）。

A2.2.5 Selcall-tone （ **5-tone** ）

- 配置 0xa1[7:0] = 8'h20 进入 5-tone 模式；

A2.2.5.1 参数配置与初始化

- 配置 0xa0[7:0] = 8'h39 ，设置 5-tone 发送调制频偏为 1.8KHz ；
- 配置 0xa4[7:0] = 8'h05 ，设置 5-tone 单次发送时长，默认 500ms ，可调节的步进长 度为 100ms ；
- 配置 0xa3[7:0] = 8'h05 ，设置 5-tone 相邻帧间隙时长，默认 500ms ，可调节的步进 长度为 100ms ；
- 配置 0xa7[7:0] = 8'h0a ，设置 5-tone 解调门限；
- 配置{ 0xaf[3:0], 0xae ， 0xad } ，设置 5-tone 发送码，由“ A ”、“ B ”、“ C ”、“ D ”、“ E ” 5 个配对组成，例如“ A-B-C-D-E ”；
- 配置 0xd3[3:0] = 4'hc ， 0xd2[7:0] = 8'h80 ，设置 5-tone 解调采样深度，默认为 3200 （ 32KHz ， 100ms ）；
- 接收解调系数配置： 与上述 2-tone 设置相同。
- 发送频率配置： 与上述 2-tone 设置 相同。

A2.2.5.2 发送与接收

- 发送： PTT 有效时，系统将保存在寄存器 0xaf[3:0], 0xae ， 0xad 中的 5-tone 码发送， 发送格式由 0xa3 ， 0xa4 指定， 5-tone 均为 single 模式，即每次只发送一遍序列码， 下次发送需等到新的 PTT 有效；

- 接收： MCU 在每次 FM 中断来临时将寄存器{ 0x95[3:0] ， 0x94 ， 0x93} 中的数据与 软件预设的 5-tone 接收地址比较，如果匹配，则打开扬声器通路（ 0x36[7:0] = 8'h72 ），反之则关闭扬声器（ 0x36[7:0] = 8'h80 ）。

B ADC 输入电压与 RSSI 值关系

低中频 450KHz 的 DMR 信号，通过 RF cable 线直接输入到 HR_C6000 的 ADC 端，通 过寄存器得到 RSSI 值与 ADC 的 I 路输入电压之间的关系如图。

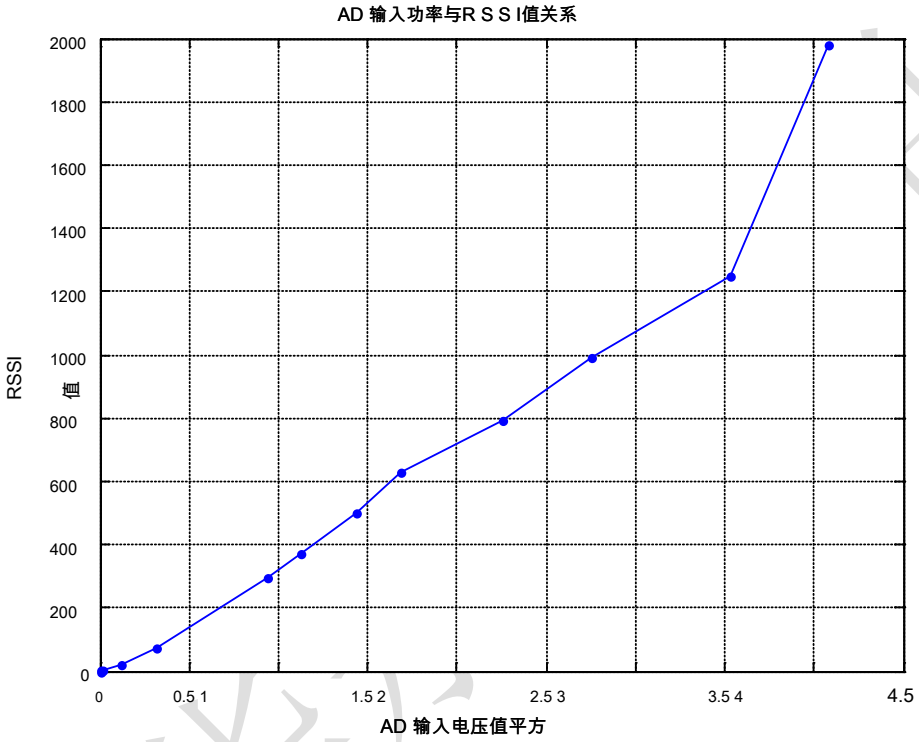


图 B.1 ADC 输入电压平方值同 RSSI 值对应关系

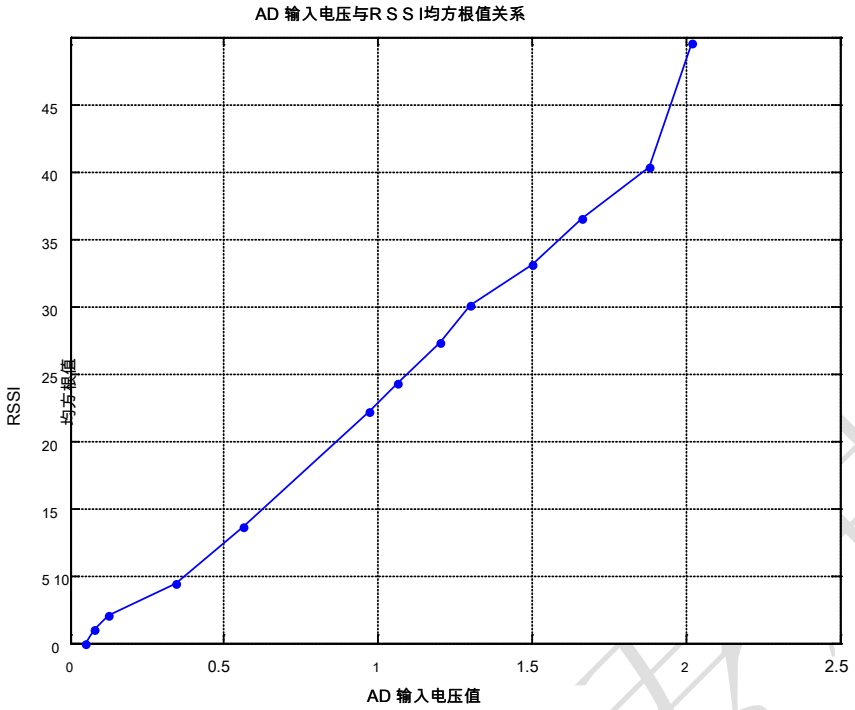


图 B.2 ADC 输入电压同 RSSI 均方根值对应关系

表 B.1 ADC 输入电压对应 450KHz 的 DMR 输入信号幅度值如下表：

输入信号幅度(dBm)	I 路单端输入电压（ V ）	RSSI 值
- 34	0.048	0
- 28	0.080	1
- 22	0.125	4
- 16	0.340	19
- 10	0.560	75
- 4	0.970	294
- 3	1.060	370
- 2	1.200	500
- 1	1.300	628
0	1.500	790
1	1.660	993
2	1.880	1250
3	2.020	1980