

TKR-830 Circuit Description

Outline

The TKR-830 is a UHF-band relay radio unit for business radio applications. It is designed as a high-performance model with enhanced basic transmit/receive functions. The TKR-830 also has the PC tune and PC monitor functions and its circuits are configured to support future upgrading flexibly.

The TKR-830 has three PLL circuits in the transmitter unit and two PLL circuits in the receiver unit. All the PLL circuits are controlled with the same basic frequency, so the transmit and receive frequencies are very stable compared with the previous models. It uses a new circuit design to modulate the transmit reference PLL and the transmit main PLL at the same time during transmission. Therefore, it features flat modulation characteristics from a low-frequency range regardless of whether the external reference frequency or the internal TCXO is used.

Transmitter circuit

The transmitter unit (X56-303- A/3) consists of (1) internal/external reference circuit, (2) transmit reference PLL circuit, (3) receive reference PLL circuit, (4) transmit main PLL circuit, (5) driver circuit, (6) modulation level adjustment circuit, and (7) other circuits.

(1) The internal/external reference circuit switches between the internal ± 1.0 ppm/20MHz TCXO X101 and the 10MHz external reference automatically. If there is no external reference input, the internal TCXO is used as the basic frequency for PLL circuits. When the external reference (10MHz/-10dBm or higher) is input to CN101, the external reference is used as the reference frequency for all PLL circuits. The circuits operate as follows.

When the external reference signal (10MHz) is input, its impedance is converted by an emitter follower (Q102). Then, harmonic components are generated by a double amplifier. Only the 20MHz component is taken by the MCF XF210 and sent to D101 and high-frequency amplifier Q205. The 20MHz signal amplified by Q205 is converted to a direct current voltage by the double-voltage detection circuit consisting of C265 and D205. The direct current voltage is compared with the reference voltage by comparator IC204. If the detected direct current voltage is higher than the

reference voltage, the comparator output changes from "L" to "H".

The comparator output switches Q110, Q111, Q112, Q113, and Q114 switching transistors. Q110 turns "OFF" and Q114 turns "ON". Switching diode D101 conducts (since Q110 is "OFF", D103 does not conduct). The 20MHz reference signal generated from the external reference signal is input to IC201 and IC202 and the external reference signal is used as the reference frequency.

When the comparator output turns Q206 "ON", the comparator reference voltage decreases by a certain level, and hysteresis characteristics are obtained. Even if the external reference level changes slightly, the comparator output does not change. If there is no external reference input, the double voltage detection circuit C265 and D205 does not output any signal, the comparator output is "L". Therefore, Q114 turns "OFF" and Q110 turns "ON". Power is supplied to the internal TCXO and D103, the internal TCXO 20MHz reference signal is input to IC201 and IC202, and the internal TCXO is used as the reference frequency. The TCXO frequency stability may be affected by the output load impedance. The TKR-830 has a MOS FET buffer amplifier Q15 to stabilize the TCXO output load impedance and its frequency.

(2) The transmit reference PLL circuit generates the reference frequency signal (19.2MHz) for the transmit main PLL and consists of IC201, X201, Q201, and Q202.

The VCO has a no-adjustment type crystal oscillator circuit (based on a Colpitts circuit) consisting of Q201 and X201, varicap D203 for modulation, and varicap D201, D202 for changing the oscillator frequency by direct current voltage.

The signal generated by the VCO is fed to buffer amplifier Q202. The signal then goes to a "pi" type LPF to remove unwanted harmonic components. The resulting signal goes to the fractional N type single-chip PLL IC (IC201), and the phase of the divided frequency (200kHz) is compared with that of the reference frequency. The phase difference signal enters the internal charge pump, is converted to an analog signal (0 to 5 V) and output from the PHA pin. Then, the signal is converted to a direct current voltage by a laglead type loop filter. The capacity of D201 and D204 is varied by the direct current voltage to keep the VCO oscillator frequency 19.2MHz.

The stabilized 19.2MHz oscillator signal is taken from the LPF output, output to IC101 Xin pin, and used as the reference frequency signal for the transmit main PLL.

(3) The receive reference PLL circuit produces the reference frequency signal

(19.2MHz) for the receive PLL (first and second local oscillator), and consists of IC202, X202, Q204, and Q241.

The VCO contains a no-adjustment type crystal oscillator circuit (based on a Colpitts circuit) consisting of Q240 and X202 and varicap D240 for changing the oscillator frequency by direct current voltage.

The signal generated by the VCO is fed to the buffer amplifier Q241. The signal then goes to a "pi" type LPF to remove unwanted harmonic components. The resulting signal goes to the fractional N type single-chip PLL IC (IC202), and the phase of the divided frequency (200kHz) is compared with that of the reference frequency. The phase difference signal enters the internal charge pump, is converted to an analog signal (0 to 5 V) and output from the PHA pin. Then, the signal is converted to a direct current voltage by a laglead type loop filter. The capacity of D240 is varied by the direct current voltage to keep the VCO oscillator frequency 19.2MHz.

The stabilized 19.2MHz oscillator signal is taken from the LPF output, output to IC101 Xin pin, and used as the reference frequency signal for the receive PLL (first and second local oscillator). The impedance is converted by emitter follower amplifier Q115. The resulting signal passes through the "pi" type LPF and goes to the receive PLL reference output pin CN102.

The unlock signals for the transmit reference PLL circuit and receive reference PLL circuit are output from pin 18 (LOCK) of IC201 and IC202. The two unlock signals are ANDed, and the reference PLL unlock signal (LDS) is sent from CN3 to the control unit.

(4) The transmit main PLL circuit generates the transmit frequency signal. This circuit consists of a clap type oscillator VCO consisting of Q1 and Q2 and single-chip PLL IC (IC101). When transmitting 450.0000 MHz to 464.995 MHz, the Q2 VCO oscillates and Q1 stops. The switching operation is performed by controlling switching transistors Q3, Q4, and Q5 using the output Q1 from shift register IC4.

The signal generated by Q1 or Q2 is fed to buffer amplifier Q6. Q6 provides isolation, and the signal goes to the high frequency amplifiers Q9 and Q107. Q107 amplifies the signal to the level required for the internal prescaler in IC101. Unwanted harmonic waves are removed by the "pi" type two-step LPE, and the resulting signal is input to IC101 Fin pin. IC101 divides the VCO oscillator signal input to Fin and the transmit PLL reference signal (19.2MHz) input to Xin by the divide ratio, and the phase is

compared with the 12.5kHz comparison frequency. The phase difference signal detected by phase comparison enters the internal charge pump, is converted to an analog signal (0 to 5 V) and output from the Do pin.

The analog signal output from the Do pin is converted to a direct current signal by the laglead type loop filter. The direct current signal is applied to varicap D1, D3, D2, D4 to lock the VCO oscillator frequency with the desired oscillator frequency. The direct current signal passes through the IC109 operational amplifier and buffer amplifier, and is output from CN3 as the voltage signal (CVT) for monitoring the transmit main PLL lock voltage.

(5) The driver circuit amplifies the transmit frequency signal generated by the transmit main PLL circuit to the level required for input to the final unit (X56-303 B/3). The driver circuit consists of high frequency amplifier Q9, high frequency switch D7, D10, high frequency amplifier Q13, high frequency amplifier Q14, direct current amplifier Q17, and switching elements Q18, Q203, Q8, Q16, Q10, Q12, and Q11. When the transmit main PLL is locked, the IC101 LD pin goes "H", and the collector of Q17 goes "L". The collector of Q18 goes "H", the collector of Q203 goes "L", and the collector of Q8 goes "H". The logic is the opposite to the logic when the transmit main PLL is unlocked.

The transmit main PLL lock signal is output to CN3 as a signal "LDT" from the collector of Q18. This signal is used for the CPU in the control unit to monitor the lock state of the transmit main PLL. (See the control unit circuit description.)

When the collector of Q8 goes "L", Q16 turns "ON" and Q11 turns "OFF" regardless of whether the base voltage of Q10 is "H" or "L". Therefore, the power 8T for the drive is not provided. When the circuit is unlocked, it is protected to inhibit transmission.

The transmitter operation is controlled according to the data sent from the CPU in the control unit to shift register IC4. When IC4 pin 5 Q2 is "L" and the collector of Q8 is "H" (the transmit main PLL is locked), Q16 and D10 turn "OFF" and Q12 and Q11 turn "ON", 8T is supplied to the drive stage, D7 turns "ON", and the transmit signal is sent to Q13.

The transmit signal level input to Q13 is about 0 dBm. Q13 amplifies it by about 10 dB, and Q14 also amplifies it by about 10 dB. 20 dBm (about 100 mW) is output from drive output connector CN1.

(6) The modulation level adjustment circuit adjusts the modulation signal level and provides specified modulation. It consists of IC105, IC3, IC100, and IC203.

IC3 is an electronic volume IC. The signaling frequency change adjustment, signaling modulation balance adjustment (transmit reference PLL and transmit main PLL are modulated at the same time to provide flat modulation characteristics), maximum sound frequency change, and the reference voltage setting for transmission power adjustment can be performed for each transmit frequency and for each channel using the FPU (KPG-47D) and a personal computer.

IC105 is a modulation signal summing amplifier (A/2) (sums the sound signal and the signaling signal whose balance is adjusted and modulates the transmit main PLL) and a signaling signal amplitude fine-adjustment amplifier (B/2).

IC203 is a DC amplifier that fine-adjusts the transmission power reference voltage generated by IC3. The "PC" signal is output to the final unit from connector CN.

(7) IC106 is an EEPROM. The transmit adjustment data adjusted for each unit is written into the EEPROM. If the unit is installed in another set, it is not necessary to adjust it again.

IC1, IC2, IC103, IC108, and IC110 are three-pin constant-voltage power supply ICs. Each circuit contains its own power IC to maintain isolation between circuits.

The final unit (X56-303 B/3) amplifies the transmission power to a specified level. This unit consists of (1) transmission power amplifier, (2) harmonic wave elimination circuit, (3) progressive wave power/reflected wave power detection circuit, (4) APC circuit, (5) abnormal temp. detection circuit, and (6) common mode unwanted radiation prevention circuit.

(1) The transmission power amplifier IC301 uses a power module S-AU50* for portable transceivers to improve its efficiency. Driver output CN1 of the transmit unit is fed to CN301 of the final unit through a coaxial cable, and enters pin 1 of transmission power amplifier IC301 through a 5dB attenuator. The transmission power amplifier IC301 amplifies the power to the level corresponding to the voltage at the power control pin (pin 2) and outputs it from the output pin (pin 4).

(2) The harmonic wave elimination circuit is a three-stage "pi" type Chebyshev type LPF consisting of L301, L302, L303, C307, C312, C315, and C316. This circuit removes harmonic wave components from the transmission power amplified by the transmission power amplifier and sends the resulting signal to the progressive wave power/reflective wave power detection circuit.

(3) The progressive wave power/reflective wave power detection circuit consists of a $1/4 \lambda$ CM coupling type detection circuit formed by a strip line and a direct current amplifier IC303. The CM coupling detection circuit detects a negative voltage corresponding to a square root of the power values of the progressive wave and reflective wave. (D306 detects progressive wave and D308 detects reflective wave.) The progressive wave voltage FWD is sent to the APC circuit and control unit in the next stage, and reflective wave voltage REV is sent to the control unit through CN302. Thermistor TH301 corrects the thermal characteristics of the detection diode and keeps the APC function stable within the operation temperature range. Transmission power passes through the strip line and is output from CN308.

(4) The APC circuit consists of differential amplifier IC302 and direct current amplifier Q301. IC302 places the transmission power setting voltage PC and progressive wave detection voltage FWD from the transmit unit to + input and - input, and outputs voltage Vd amplified according to the difference between the voltages. (If $PC > FWD$, Vd increases, and if $PC < FWD$, Vd decreases.) The voltage Vd is applied to direct current amplifier Q301 in the next stage. The voltage is converted to output voltage Vg to control the power control pin (pin 2) of the transmission power amplifier IC301. At the power control pin, the transmission power increases when the voltage Vg increases, and decreases when Vg decreases. A loop is formed between transmission power, FWD, Vd, and Vg, and the transmission power converges into the point where the transmission power setting voltage PC and progressive wave detection voltage FWD are equal. The transmission power can be controlled according to the transmission power setting voltage PC. The +B voltage is applied to the power pin (pin 3) of the transmission power amplifier IC301 even when the final unit is not in transmit mode. When the voltage Vg is applied to the power control pin, the current flows to the power pin of IC301. In this case, there may be some problems, such as no isolation of the input and output of IC301. To prevent this problem, the switching transistors Q304 and Q305 are switched by transmission power 8T input through CN302 and the Vd voltage is grounded when transmission is not made.

(5) The abnormal temp. detection circuit consists of thermal switch TS301 and digital transistor Q302. This circuit reduces the transmission power amplifier function and prevents temp. rise to protect the circuits when the final unit temp. rises excessively and the circuits cannot be operated safely. This circuit rarely activate during normal use. When the thermal switch detects the operating temp., the internal switch of the thermal switch conducts. When the voltage is applied to the base of Q302, digital transistor Q302 turns "ON". The collector of digital transistor Q302 grounds the differential amplifier output voltage Vd of the APC circuit to reduce transmission power.

(6) Common mode unwanted radiation prevention circuit. The TKR-830 has a filter L304 in the power line in the final unit to reduce unwanted radiation in common mode from the power cable.

Receiver Circuit

The receiver unit (X55-304) consists of (1) front-end circuit, (2) narrow IF circuit, (3) wide IF circuit, (4) first oscillator PLL circuit, (5) second oscillator PLL circuit, (6) base band circuit, and (7) other circuits.

(1) The front-end circuit consists of helical BPF L3, high frequency amplifier Q7, helical BPF L16, mixer DBM A1, and IF switching circuit D10. The receive signal coming through CN1 goes to helical BPF L3. Unwanted signal components are damped and only the necessary band (about 5MHz) signal is sent to the high frequency amplifier Q7. The operating point of Q7 is set to maximize the gain and minimize distortion. The helical BPF L16 removes the unwanted out-of-band high frequency components produced by high frequency amplifier Q7 and unwanted components leaked from the previous circuits, and sends only the necessary signal to mixer DBM A1. The mixer DBM A1 mixes the first local oscillator signal generated by the first local oscillator PLL with the receive signal coming from the helical BPF L16 to produce a first IF signal (73.05MHz). The first IF signal is switched to the narrow or wide IF circuit by the switching diode D10.

(2) The narrow IF circuit consists of two-pole MCF XF2, four-pole MCF XF4, IF amplifier Q25, IF amplifier Q32, FM detection IC IC7, ceramic filter CF1, and CF3. The unwanted components of the first IF signal connected to the narrow IF circuit by the switching diode D10 are removed by the overtone type two-pole MCF XF2. The resulting signal is amplified by IF amplifier Q25. Unwanted signal components are further eliminated by the overtone type four-pole MCF XF4 to maintain three-signal characteristics. The first IF signal output from XF4 is amplified by IF amplifier Q32 and input to pin 24 of FM detection IC IC7. The FM detection IC mixes the second PLL local oscillator signal with the first IF signal to generate a second IF signal (450kHz). Unwanted components of the second IF signal are removed by ceramic filter CF1. The resulting signal is amplified by the IF amplifier in IC7. Unwanted components of the amplified signal are further removed by ceramic filter CF3 to improve the two-signal characteristics of the IF stage. The signal then enters the quadrature detection circuit. The signal with a phase shifted 90 degrees by phase shift coil L53 is compared with the original signal waveform to perform FM detection and generate the base band signal. The base band signal is output from pin 15 of IC7 and enters the low frequency amplifier IC11 (A/2 and B/2). The signal amplified by IC11 (A/2) goes to the Y0 input of multiplexer IC9 and the V2 input of electronic volume IC9. The level of the signal that enters V2 of the electronic volume IC is adjusted, the signal passes through the hysteresis circuit AF switch Q34. The signal goes to IC7 noise filter input (pin 17), and high frequency components are removed by a HPF. The signal is noise-detected and compared, and the noise squelch signal (N-DET) is fed to DC switch Q36. The voltage signal (RSSI) corresponding to the IF signal strength from the two second IF amplifiers in IC7 are compared with the reference voltage set by electronic volume V4 by the internal RSSI comparator, and the RSSI squelch signal (C-DET) is output from pin 20 of IC7. C-DET enters DC switch Q37 and is ANDed with N-DET by DC switch Q38. A squelch signal (SC) is output from connector CN6.

(3) The wide IF circuit consists of two-pole MCF XF1, four-pole MCF XF3, IF amplifier Q24, IF amplifier Q31, FM detection IC IC8, ceramic filter CF2 and CF4. The unwanted components of the first IF signal connected to the wide IF circuit by the switching diode D10 are removed by the overtone type two-pole MCF XF1. The resulting signal is amplified by IF amplifier Q24. Unwanted signal components are further eliminated by the overtone type four-pole MCF XF3 to maintain three-signal

characteristics. The first IF signal output from XF3 is amplified by IF amplifier Q31 and input to pin 24 of FM detection IC IC8. The FM detection IC mixes the second PLL local oscillator signal with the first IF signal to generate a second IF signal (450kHz). Unwanted components of the second IF signal are removed by ceramic filter CF2. The resulting signal is amplified by the IF amplifier in IC8. Unwanted components of the amplified signal are further removed by ceramic filter CF4 to improve the two-signal characteristics of the IF stage. The signal then enters the quadrature detection circuit. The signal with a phase shifted 90 degrees by phase shift coil L52 is compared with the original signal waveform to perform FM detection is performed and generate the base band signal. The base band signal is output from pin 15 of IC8 and enters the low frequency amplifier IC12 (A/2 and B/2). The signal amplified by IC12 (A/2) goes to the Y1 input of multiplexer IC and the V1 input of electronic volume IC9. The level of the signal that enters V1 of the electronic volume IC is adjusted, and the signal passes through the AF switch Q35. The signal goes to IC8 noise filter input (pin 17), and high frequency components are removed by a HPF consisting of external CRs. The signal is noise-detected and compared, and the noise squelch signal (N-DET) is fed to DC switch Q36. The voltage signal (RSSI) corresponding to the IF signal strength from the two second IF amplifiers in IC8 are compared with the reference voltage set by electronic volume V3 by the internal RSSI comparator, and the RSSI squelch signal (C-DET) is output from pin 20 of IC8. C-DET enters DC switch Q37 and is ANDed with N-DET by DC switch Q38. A squelch signal (SC) is output from connector CN6. The C-DET signal and N-DET signal are the same for both the wide and narrow IF circuits. (The wide and narrow IF circuits do not operate at the same time.)

(4) The first local oscillator PLL circuit consists of clap type VCO consisting of Q8 and Q9, fractional N type single-chip PLL IC IC1, buffer amplifier Q14, and high frequency amplifier Q3, Q1, Q5, and Q6. The first local oscillator is a lower hetero local oscillator with a receive frequency of 450.0000 to 480.0000 MHz. The VCO oscillator frequency is 376.95 to 406.95 MHz. One of the two VCOs, Q8, covers the range of 376.95 to 391.945 MHz, and Q9 covers the range of 391.95 to 406.95 MHz. One of the VCOs is selected by switching switching transistors Q10, Q12, and Q13 by shift register IC3 output (Q3.) The signal generated by Q8 or Q9 is fed to buffer amplifier Q14. The signal is isolated and is sent to high frequency amplifiers Q3 and Q23.

The signal input to Q23 is amplified to the level required for IC1 prescaler input, harmonic wave components are removed by a "pi" type two-step LPE and the resulting signal goes to pin 5 of IC1. PLL IC IC1 divides the CN7 receive PLL reference signal 19.2MHz coming from the transmitter unit and the signal generated by the VCO and compares phases with a comparison frequency of 12.5 kHz. The detected phase difference signal is fed to the internal charge pump, converted to an analog signal (0 to 5 V), and output from the PHP pin. The analog signal output from the PHP pin is converted to a direct current voltage by a laglead type loop filter. The capacity of varicaps D2, D3, and D4 is varied by this direct current voltage to lock the VCO to the desired oscillator frequency. The signal input to Q3 is amplified to about 20 dBm by high frequency amplifier Q3, Q4, Q5, and fed to mixer DBM A1 as a first local oscillator signal.

(5) The second local oscillator PLL circuit consists of PLL IC IC15, crystal oscillator X1, oscillator FET Q21, buffer amplifier Q23, high frequency amplifier Q15, Q30, Q33, and emitter follower Q27. The VCO consists of no-adjustment type crystal oscillator circuit (Q21 and X1) (based on a Colpitts oscillator circuit) and varicap D9. The signal generated by the VCO is fed to buffer amplifier Q23. The signal is isolated by Q23 and fed to high frequency amplifier Q15 and emitter follower amplifier Q27. High frequency amplifier Q15 amplifies the signal to the level required for IC15 prescaler input, and outputs it to IC15 Fin (pin 20). IC15 divides the CN7 receive PLL reference signal 19.2MHz coming from the transmitter unit and the VCO-generated signal input to Fin and compares phases with a comparison frequency of 200 kHz. The detected phase difference signal is converted to an analog signal (0 to 5 V) by the internal charge pump. The signal is output from the IC15 Do pin, and converted to a direct current voltage by a laglead type loop filter. The VCO varicap D9 is controlled by the direct current voltage to lock stably with the desired frequency 72.6 MHz. The signal input to emitter follower amplifier Q27 is isolated, and moved from the Q27 emitter to high frequency amplifier Q33, Q30. The signal is amplified to the level required for FM detection IC OSC1 input, and output to the OSC1 pin of each FM detection IC. The unlock detection signals from the two PLL circuits in the receiver unit are ANDed by IC18, and the resulting signal is sent to the CPU in the control unit from CN6 as receive PLL lock signal LDR.

(6) The base band signal circuit consists of HPF Q26 and Q28, switching diode D11, and digital transistor Q29. The level of the base band signal detected by the narrow and wide FM detection circuits is adjusted by the amplifier (B/2) of IC11, IC12. The active detection output is selected by Z0 and Z1 of multiplexer IC6. The amplified base band signal is output to CN6 from IC6 "Z" pin as the DET signal. The level is adjusted by the amplifier (A/2) of IC11, IC12 and the active detection output is selected by Y0 and Y1 of multiplexer IC6. The subaudio band components of the signal output from the "Y" pin are cut by the HPF of Q26 and Q28, the signal is switched by the squelch signal by D11 and Q29, and output from CN6 as the RA signal.

(7) The receiver circuit contains an EEPROM (IC10) like the transmitter circuit. Adjustment data for each unit is written into the EEPROM when adjustment ends. Therefore, even if the unit is moved to another set, no adjustment is required. IC2, IC4, IC13, IC16, and IC17 form a three-pin constant voltage power supply IC. Each circuit contains a power supply to isolate circuits. Q17 is a ripple filter for the power supplied to the first local oscillator PLL VCO. The RSSI signal for the active wide or narrow FM detection IC is selected by "X1, X0, X" of the multiplexer IC6. The signal is output from connector CN6 through the operational amplifier buffer amplifier IC (A/2). IC3 is a shift register. IC3 switches between the two IF circuit power supplies and between the second local oscillator PLL strobe data and the first local oscillator PLL VCO according to the data from the CPU. Q16, Q18, Q19, Q20, and Q22 compose a switching transistor. It controls power supplies 8CN and 8CW for the two IF circuits.

Control Circuit

The control unit (X53-381) consists of (1) CPU, (2) receive audio filter circuit, (3) LSD filter circuit, (4) AF PA circuit, (5) microphone amplifier circuit, (6) noise squelch circuit, (7) display circuit, (8) channel setting circuit, (9) RS-232C circuit, (10) external equipment connection circuit, and (11) other circuits.

(1) The CPU (IC10) is a single-chip microcomputer containing a 1Mbit flash ROM (128k x 8). The firmware can be modified easily. The CPU controls the transmitter unit, the receiver unit, the control unit, and the display circuit and transfers data to or from external devices.

(2) The receive audio filter circuit consists of operational amplifiers IC3 and IC5. The RA signal from the receiver unit (receive audio signal filtered by the receiver unit) passes through the second HPF ($f_c=300$ Hz) in IC3 (A/2) and the twin T type notch filter ($f_0=3$ kHz) in IC3 (B/2) to attenuate the signaling signal components under 300 Hz and prevent leakage of the signaling signal to the monitor audio. IC15 LFP ($f_c=3$ kHz) cuts the high frequency noise by low frequency pass characteristics. The signal passes through the volume adjustment variable resistor VR301 and goes to the AF PA circuit as the RAF signal. Its level is adjusted by V1 of electronic volume IC104, the signal passes through the operational amplifier IC105 (A/2) and is output from the CN19 D-sub 25-pin connector as the RA signal.

(3) The IC11 LSD filter circuit is a prefilter required to process the receive signal LSD (low speed data) by CPU IC10 for future upgrading. The TKR-830 does not use it.

(4) The IC8 AF PA circuit is an AF amplifier for driving speakers to monitor receive audio signals. The 4W audio output can be provided to the external speakers when power supply voltage 13.8 V/4 ohms is supplied by the 15-pin test connector "SPO.SPG" on the rear panel. The output impedance of the internal speaker is adjusted to provide an audio output of about 0.2 W when the internal speaker installed on the TKR-830 front panel is used.

(5) The display circuit contains 7-segment LED D212, D213 (orange: see the operation manual for details of display), D203 (green: power supply), D201 (red: transmission), D202 (green: busy), two-color LED D210 (green: internal/red: external reference state) to display channels and states.

(6) The noise squelch circuit in the control unit is a pulse count type noise squelch circuit designed for future upgrading. The operational amplifier IC2 (A/2) HPF and IC2 (B/2) inverting amplifier convert high frequency noise components to pulse signals. The CPU counts the pulses to operate noise squelch. The TKR-830 does not use this circuit.

(7) The microphone amplifier circuit process the audio signal when modulating from

the local microphone on the TKR-830 front panel or from the TA pin of the D-sub connector on the rear panel. It consists of AGC amplifier IC13 (B/2), Q7, HPF IC13 (A/2), amplifier Q4, twin T BEF IC5 (B/2), preemphasis/limiter (B/2), and splatter filter IC4. The audio signal coming from J201 of the local microphone passes through CN17 pin 25 (MI) and goes to the AGC amplifier IC13 (1/2), Q7. The audio signal is amplified and the gain is automatically controlled. The signal is then fed to "XO" of multiplexer IC7. (IC7 is controlled according to data from the CPU. When the local microphone is used, "XO" and "X" conduct.) The audio signal input to "XO" is output from "X" to the amplifier Q4. Q4 fine-adjusts the amplitude of the audio signal. The signal passes through the HPF, twin T BEF, preemphasis/limiter, and splatter filter. The HPF and twin T BEF damp the components under 300 Hz with the $f_c=300$ Hz high pass characteristics and $f_0=210$ Hz notch characteristics to prevent blocking by the signaling audio signal. The preemphasis/limiter circuit gives the audio signal of 300 Hz to 3 kHz +6dB/octav frequency characteristics and emphasizes high frequency to improve the signal-to-noise ratio. The limiter circuit limits the amplitude. The splatter filter attenuates high frequency components and prevents spreading of the occupied frequency bandwidth by the high frequency audio signal. The splatter filter circuit contains two Chebyshev secondary filters to provide $f_c=3$ kHz and the damping characteristics of -24 dB/octave. The audio signal processed by the microphone amplifier is output from connector CN2 to the transmitter unit as modulation signal "MOD". When the signal is modulated from the TA pin of the D-sub 25-pin connector, the audio signal TA is amplified by the amplifier IC106 (A/2), and its level is adjusted by V5 of the electronic volume IC104. The signal passes through "YO", "Y", and "XI" of multiplexer IC7 and is output to "X". The route of the signal after "X" is the same as that for the local microphone.

(8) The channel setting circuit consists of DIP switch S1, S2, and multiplexer IC107, IC108. Channels 1 to 32 can be selected according to the 5-bit data of DIP switch S1, S2 or the 5-bit data input from the D-sub 25-pin connector. One of the data is selected for channel setting according to the logic of the I/E pin of the D-sub 25-pin connector on the rear panel. If I/E is "H", the internal switch is selected. When it is "L", the external data is selected.

(9) The RS-232C circuit connects the RS-232C serial port of the personal computer

directly to the TKR-830 to perform FPU operation. The FPU can also be operated by connecting a programming cable (KPG-46) to the local microphone on the front panel. When the D-sub connector on the rear panel is used, the programming cable is not required. The 232C driver IC (IC14) changes TTL-232C levels. The FPU (KPG-47D) has a new transmitter/receiver circuit monitor function (transmission: transmission progressive power display, transmission reflective power display, transmit main PLL lock voltage display; reception: RSSI display, receive main PLL lock voltage display). Data required for this function is also transferred through RS-232C. The firmware can only be modified by the local microphone on the front panel.

(10) The external equipment connection circuit has CN19 for RS-232C: RXD2/TXD2, external modulation input: TD (signaling)/TA (audio), receive output: RD (signaling + audio)/RA (audio), speaker mute input: SPM, monitor control input: MON, transmission input: PTT, squelch output: SC, channel control: IN/EXT SW, and external channel input: EC1/EC2/EC3/EC4/EC5. CN20 has receive output: RD (signaling + audio), receive signal strength output: RSSI, transmit main PLL lock voltage output: TXCV, receive first local oscillator PLL lock voltage output: RXCV, voltage check output: VC, transmit progressive power value output: FWD, and reference frequency display output: EXTREF.

(11) IC1, IC6, IC200, IC201, and IC202 form a three-pin constant voltage power supply IC. It provides power to the control unit circuits. IC101, IC102, and IC103 form a logic IC used to switch the banks of the flash ROM. IC9 is a shift register that shifts the clock, performs AF mute, and controls the multiplexer IC according to the data from the CPU. IC109 is a NAND logic IC. This IC NANDs the AF mute signal from IC109 and the mute signal SPM from CN19 and turns Q2 "ON" or "OFF" to control muting of the input signal of the AF PA. IC204, IC205, and IC206 compose a shift register that controls display according to the data from the CPU.